Implementing design and testbench by Xilinx Vivado and SystemVerilog

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Install Xilinx Vivado

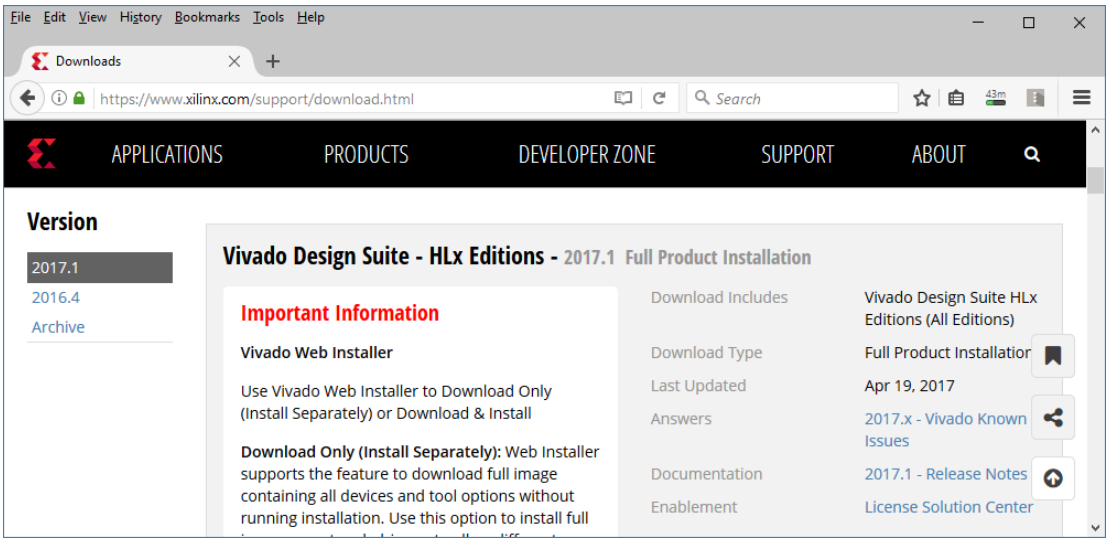
If you are at the laboratory at Ta Quang Buu library building, the software is available.

Just run the command below

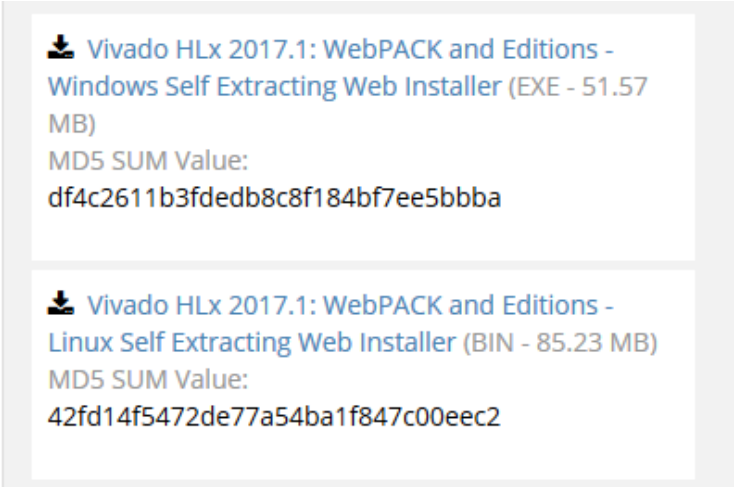
```
$ /opt/Xilinx/Vivado/2017.1/bin/vivado
```

Otherwise, you could download and install Vivado:

1. Create an free account at www.xilinx.com
2. Open URL: https://www.xilinx.com/support/download.html



3. Scroll down to the middle and click **suitable installation package link**, for Windows or for Linux (all CentOS, Ubuntu… are okay)

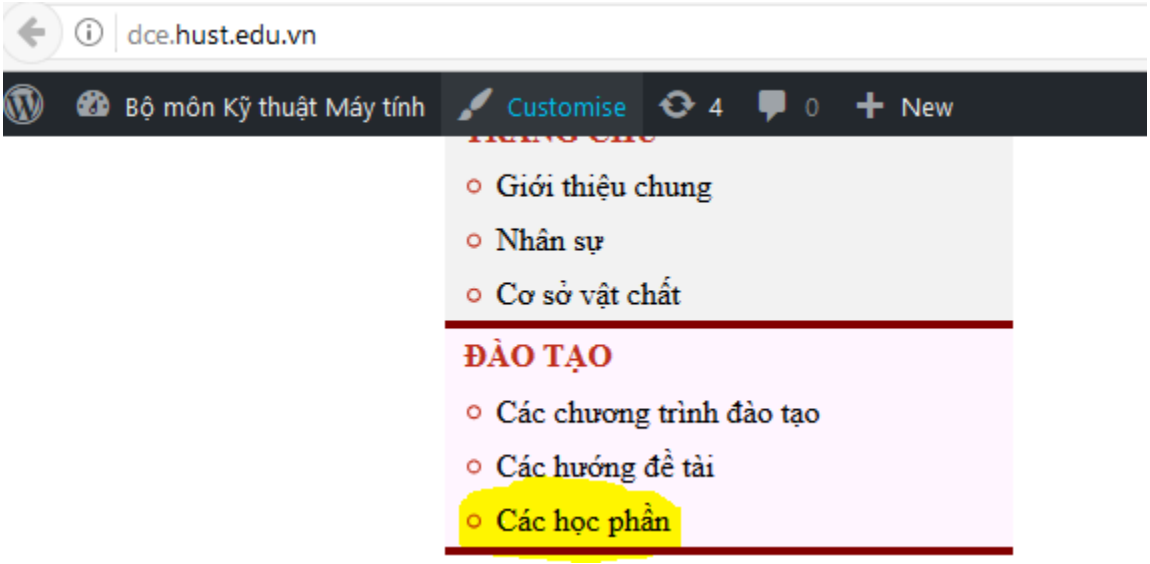


4. Install Vivado. It may take a few hours.
   Remember that: you should choice WebPack version. It's free licensing.

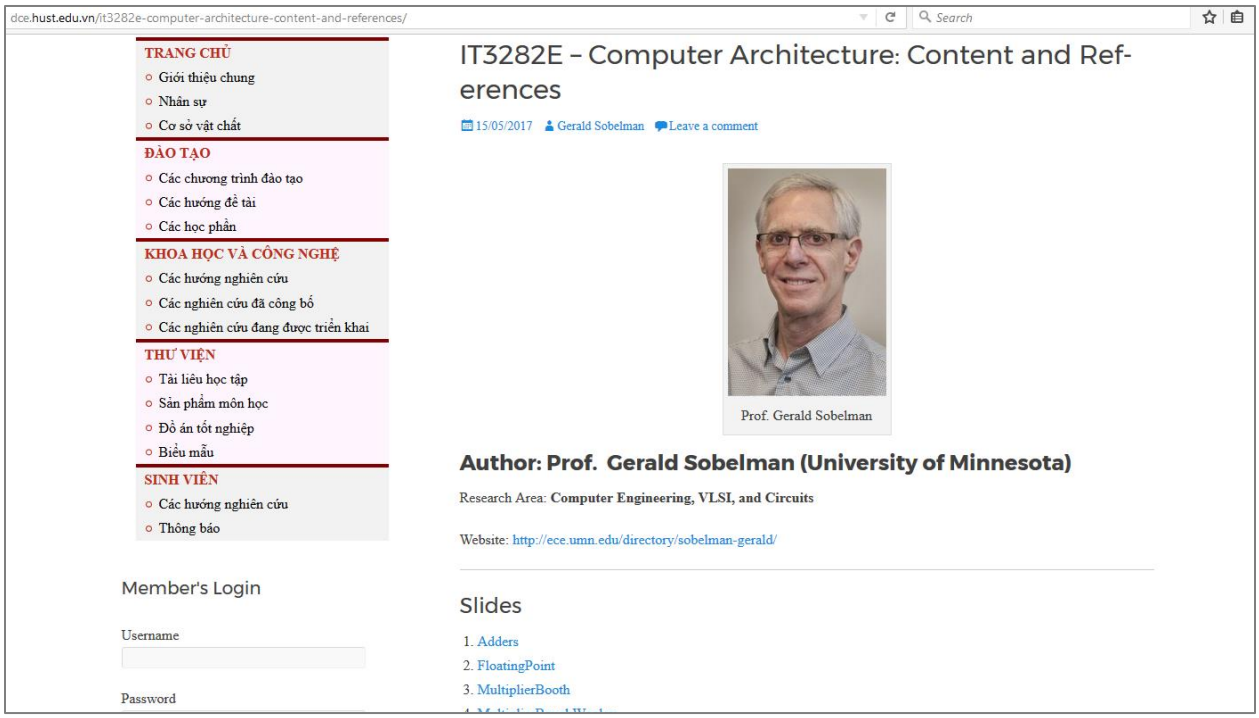
Download Resources

Download slides and Verilog files

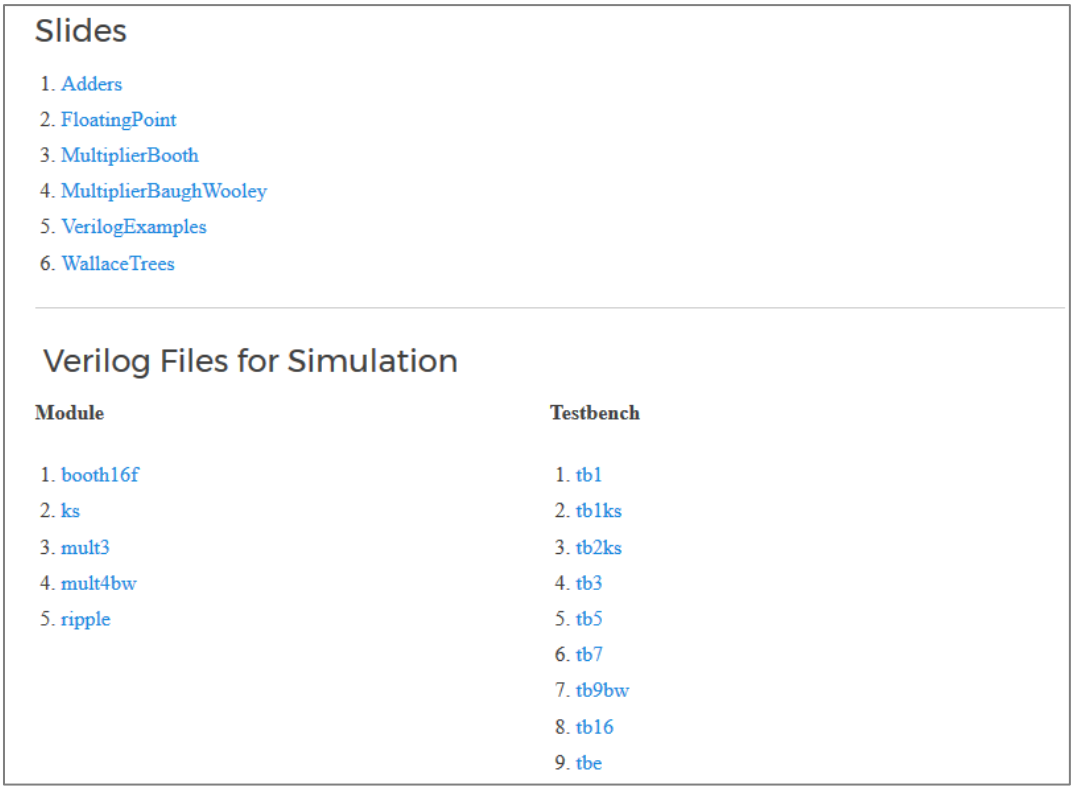
1. Open URL: http://dce.hust.edu.vn
2. At the left menu, click **Các học phần**



3. Open the post **IT3282E – Computer Architecture: Content and References**



4. Download slides and verilog files



Create Project and add Verilog sources

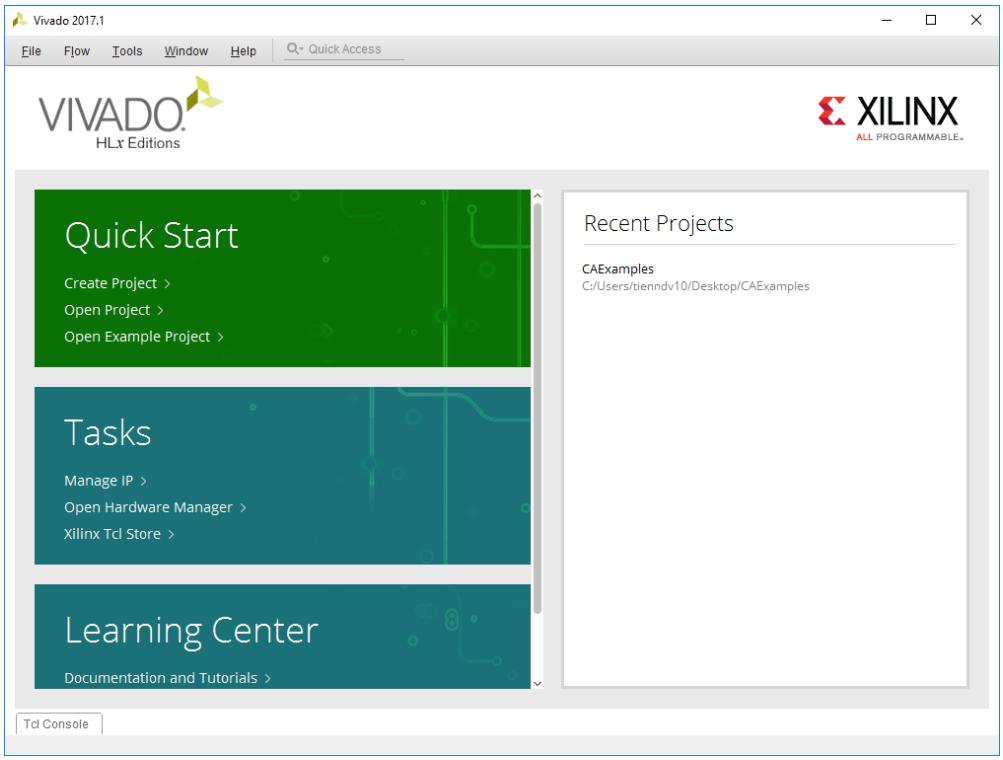
Create Project

1. Run Vivado

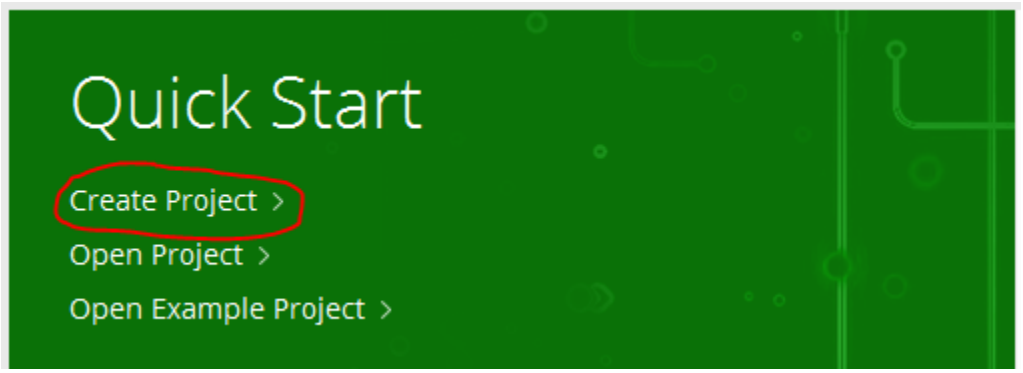
   Linux:

```
$ /opt/Xilinx/Vivado/2017.1/bin/vivado
```

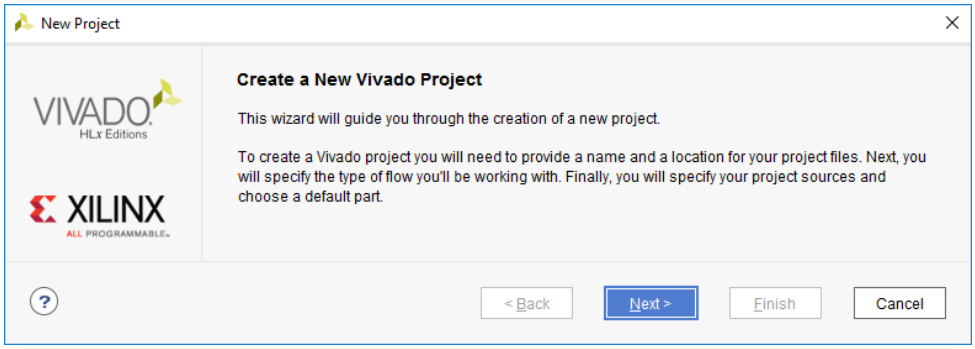
   Windows: click **vivado icon**.



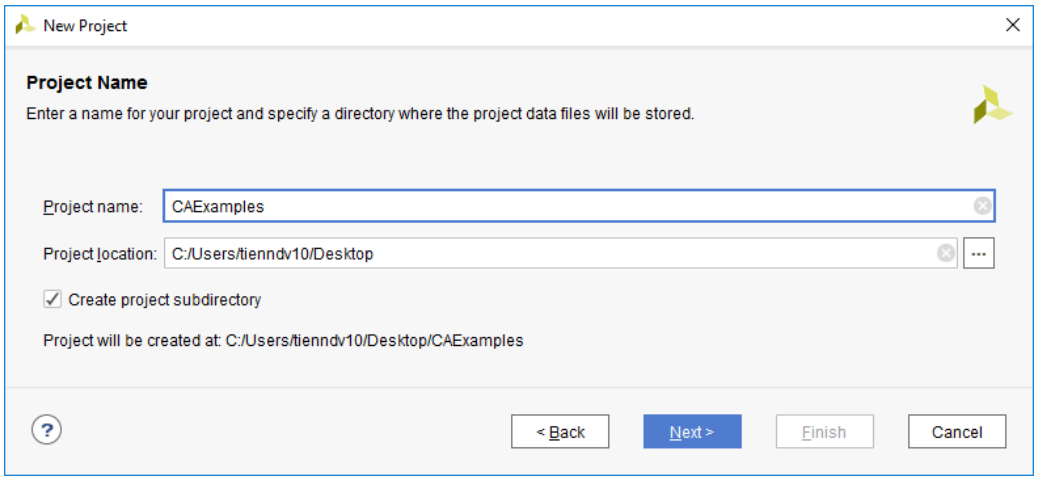
2. Click **Create New Project.**



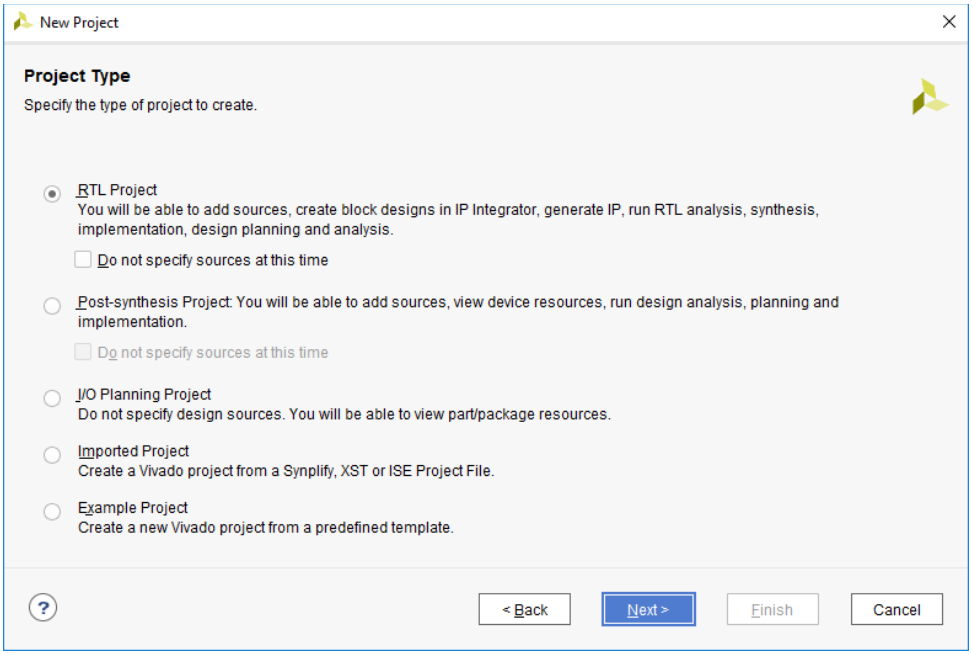
3. Click **Next**.



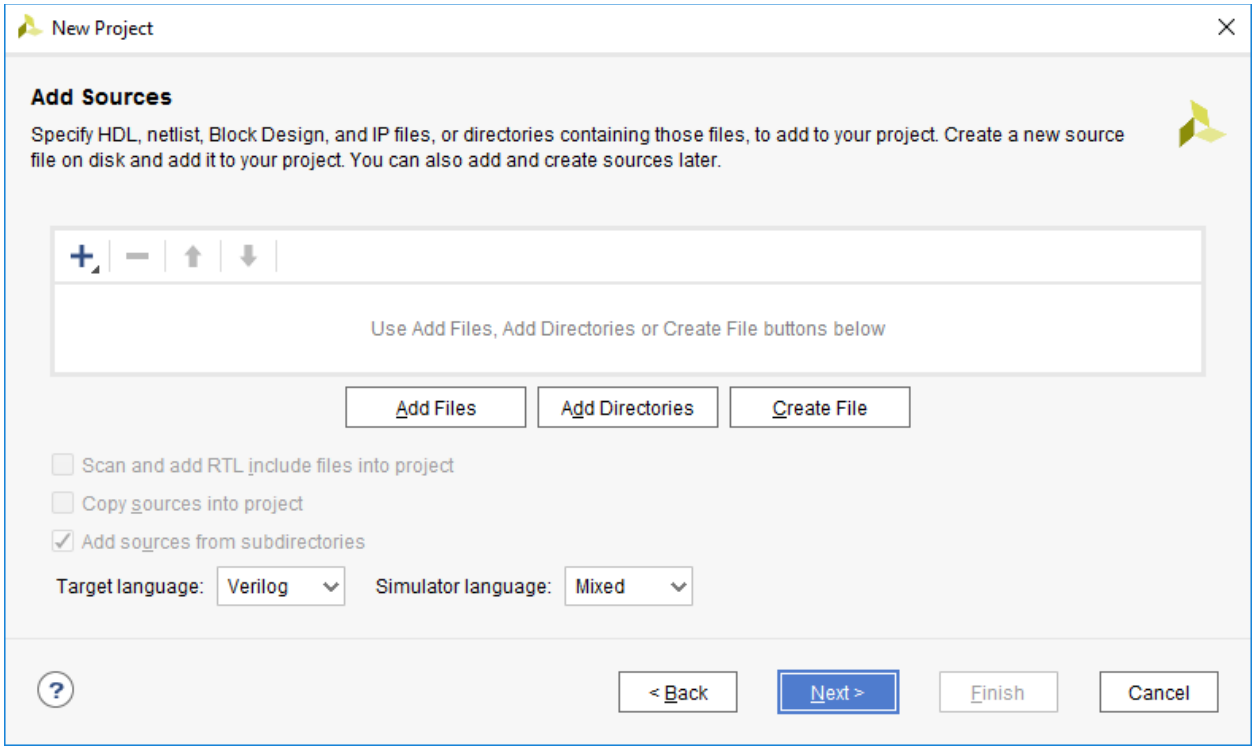
4. Name the project, for example CAExamples. Click **Next**.



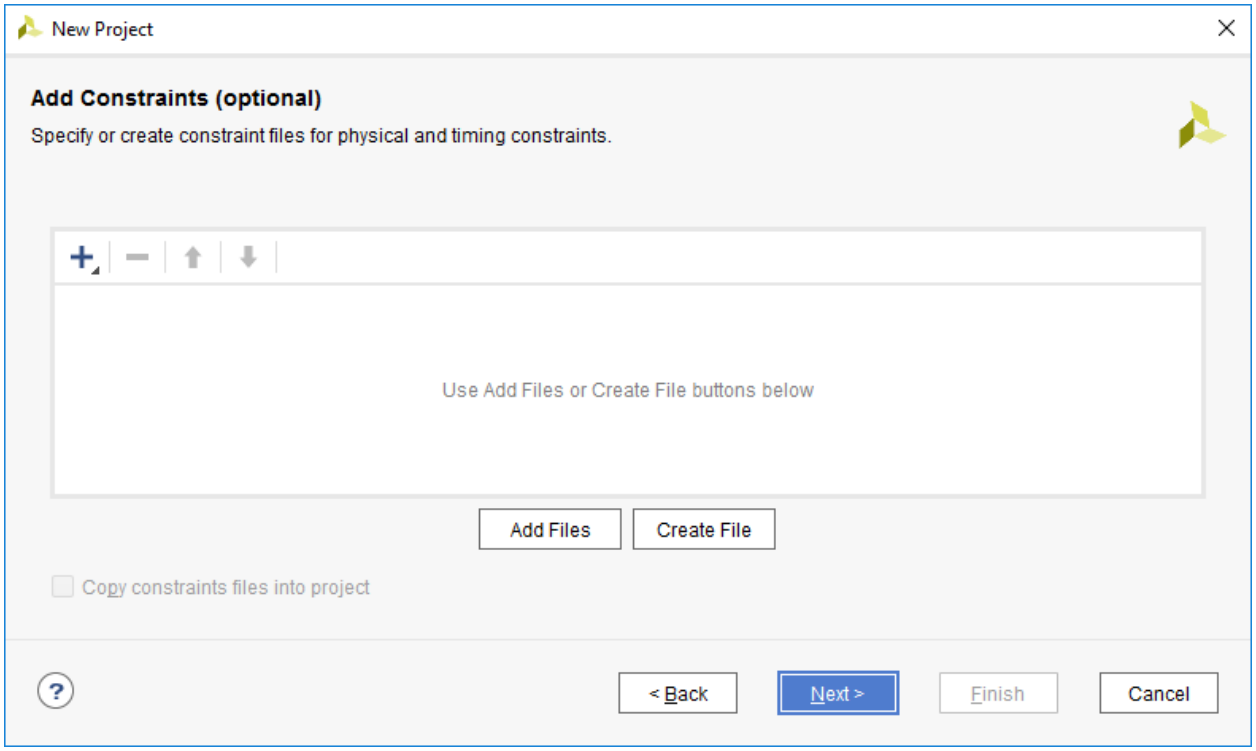
5. At New Project dialog, make sure that **RTL Project** is selected, and don't choice **Do not specify sources at this time.** Click Next.



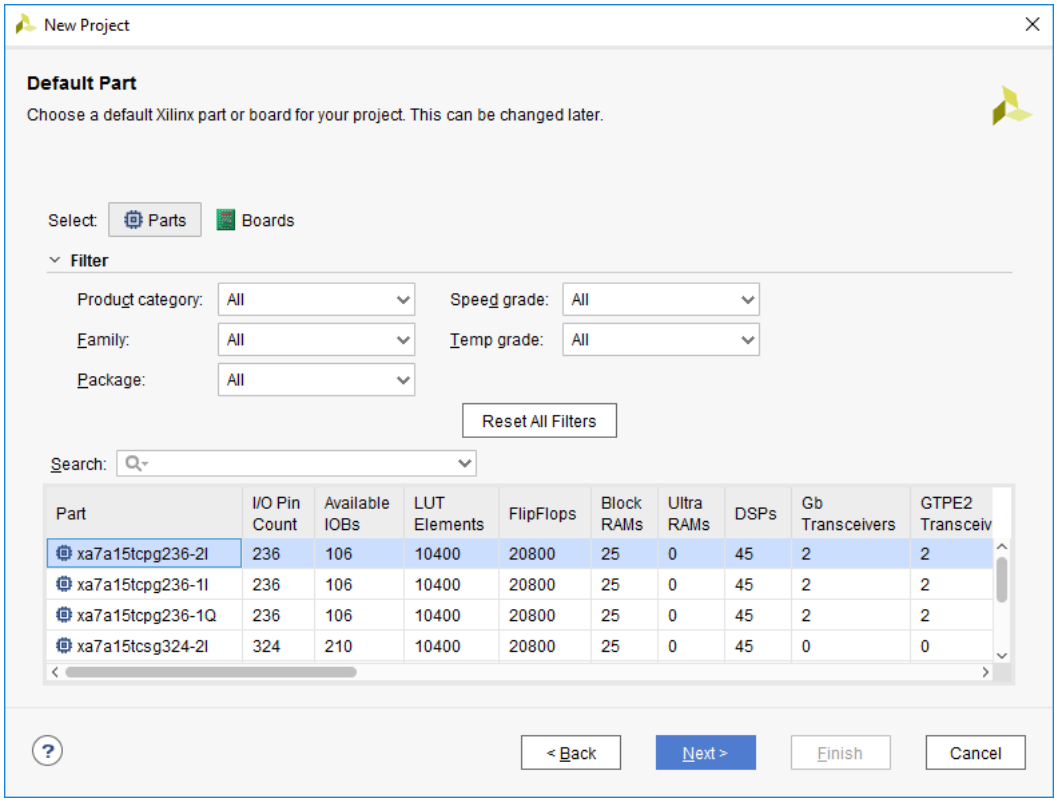
6. Target language should be **Verilog**. Click **Next**.



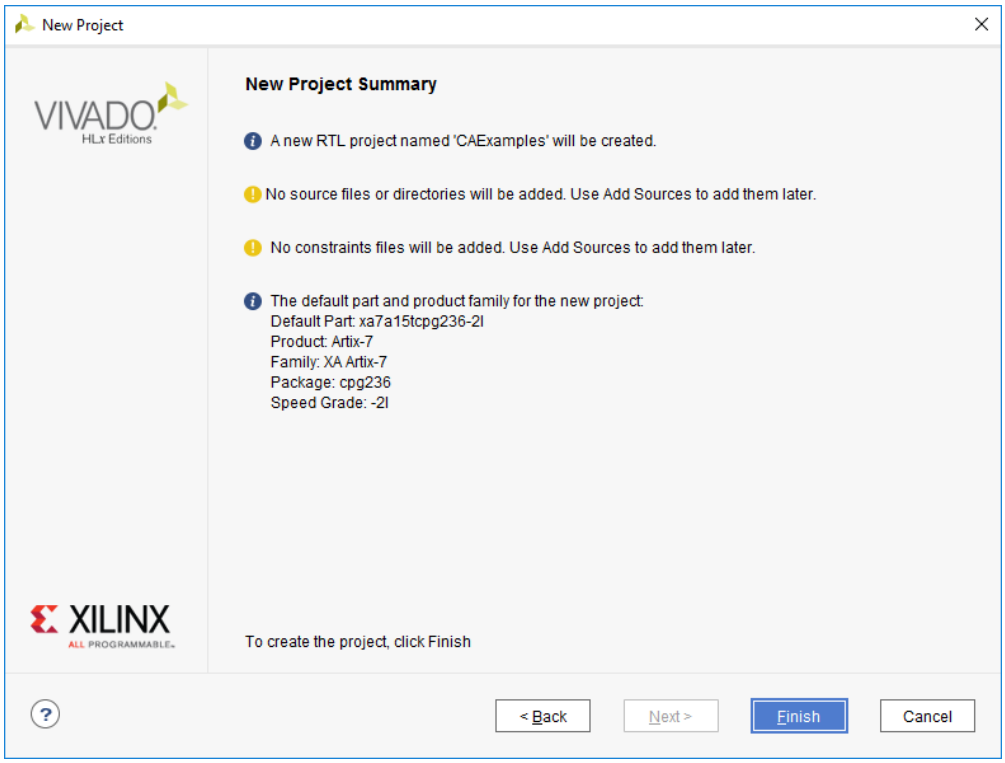
7. Click **Next**.



8. Choice a certain FPGA, for example xa7a15tcpg236-2l. Click **Next**

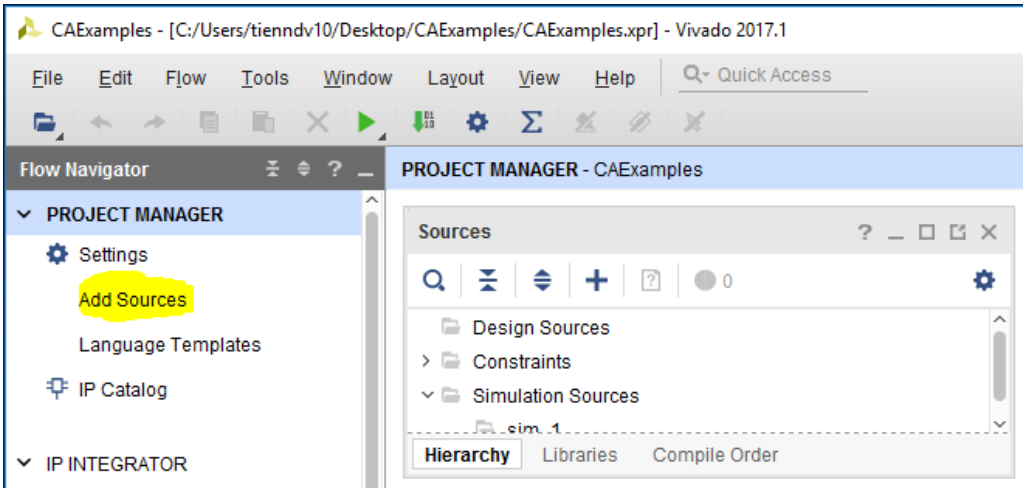


9. Click **Finish.**

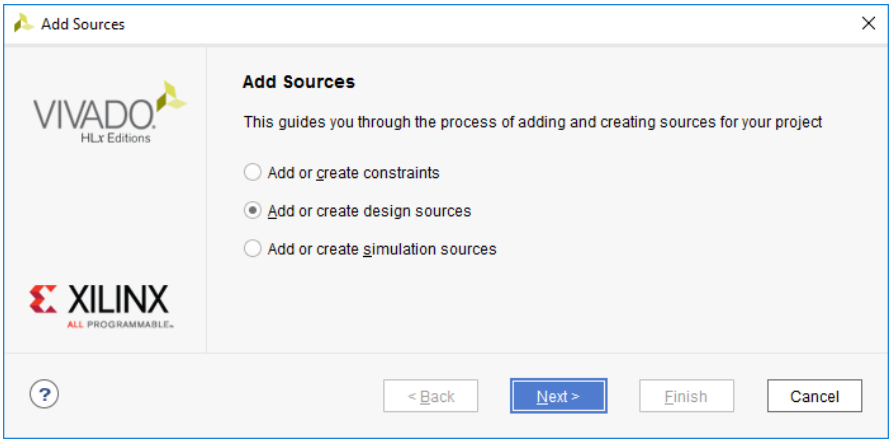


Add Verilog sources

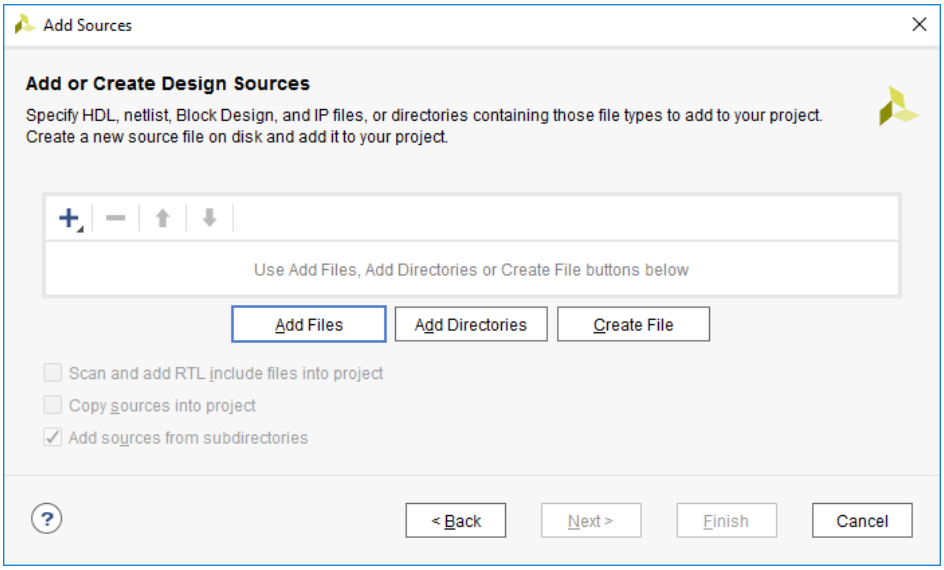
1. In the **Navigator** windows, click **Add Sources**.



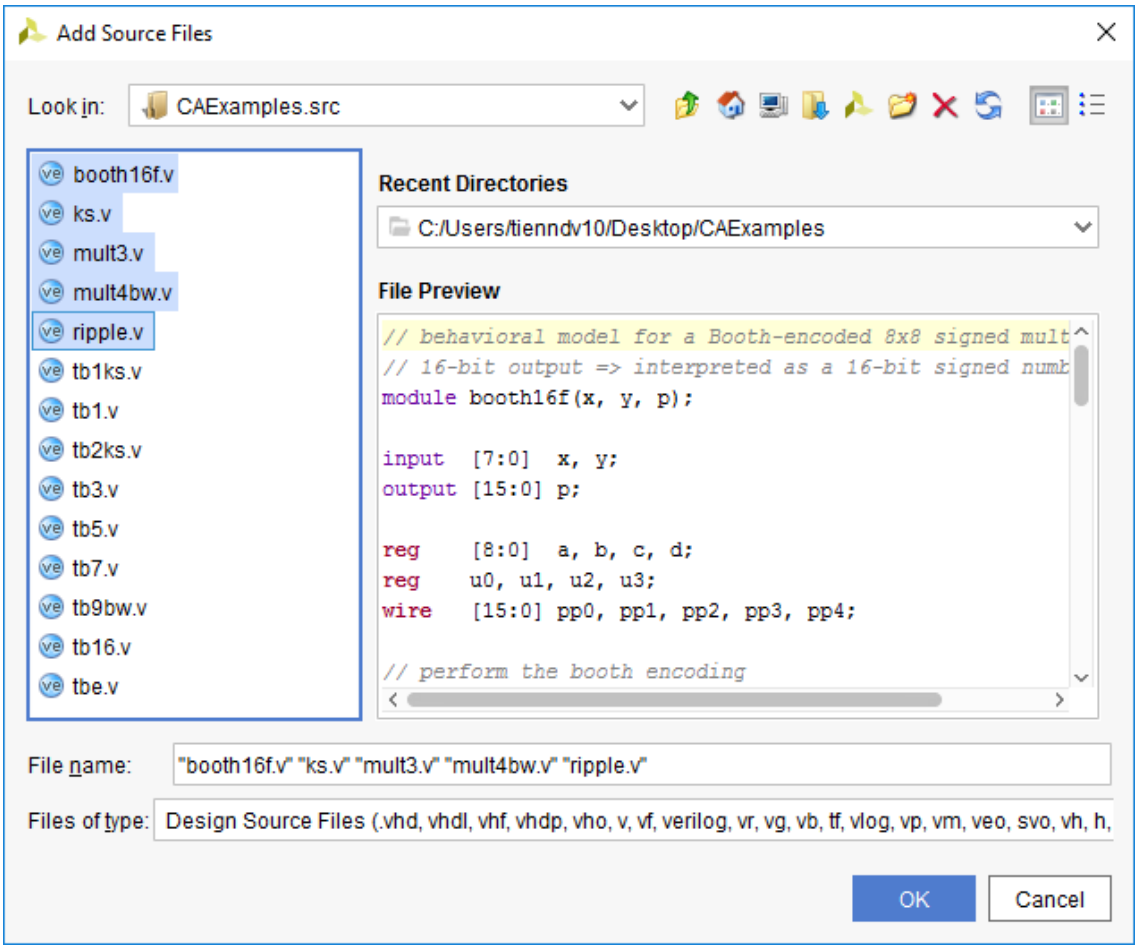
2. Select **Add or create design sources**. Click **Next**.



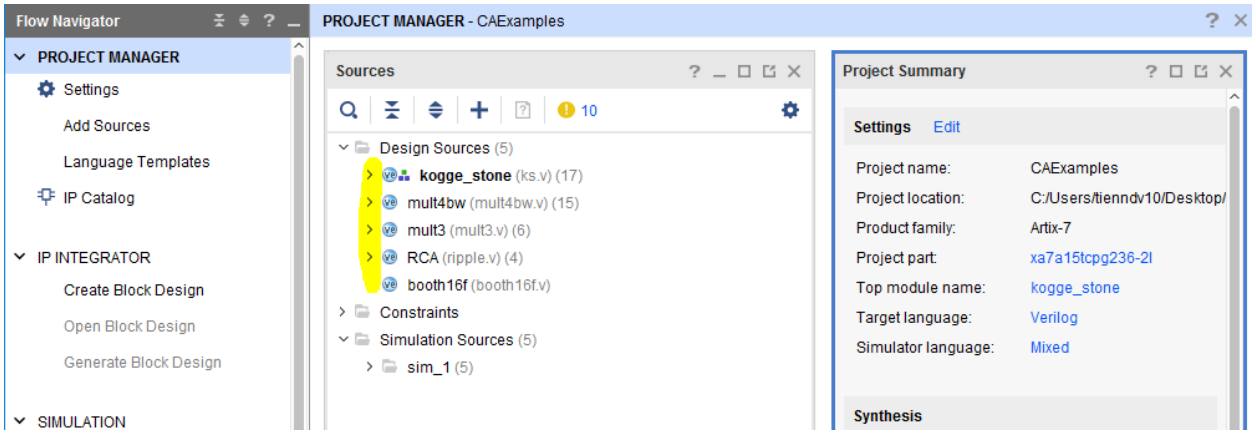
3. Click **Add Files**.



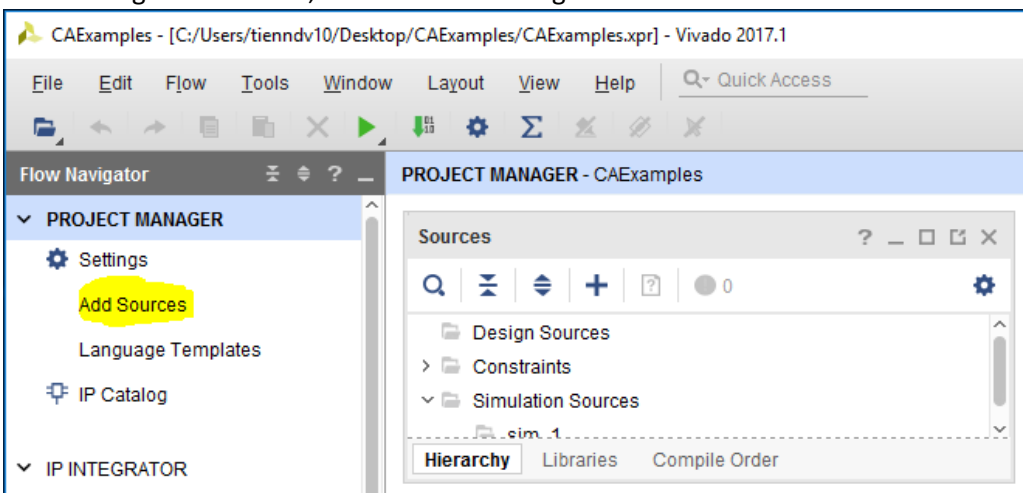
4. Select all module files you has downloaded, except testbench files (tb….v). Click **OK**.



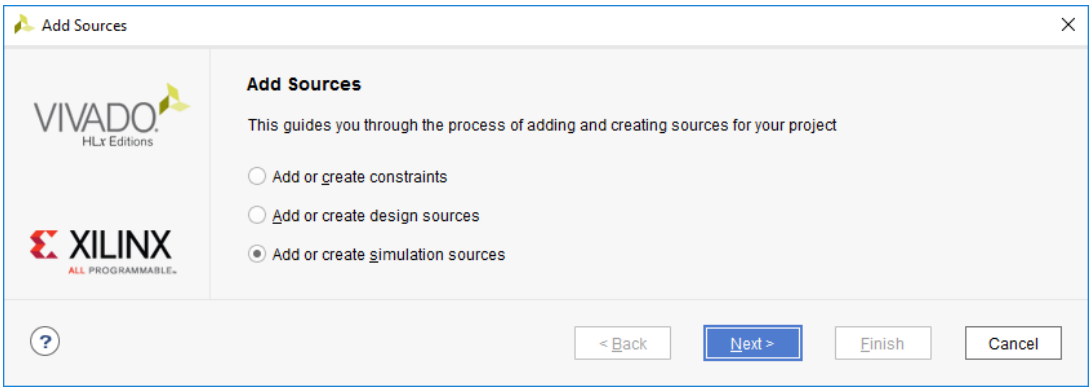
5. Click **Finish**. The project as below



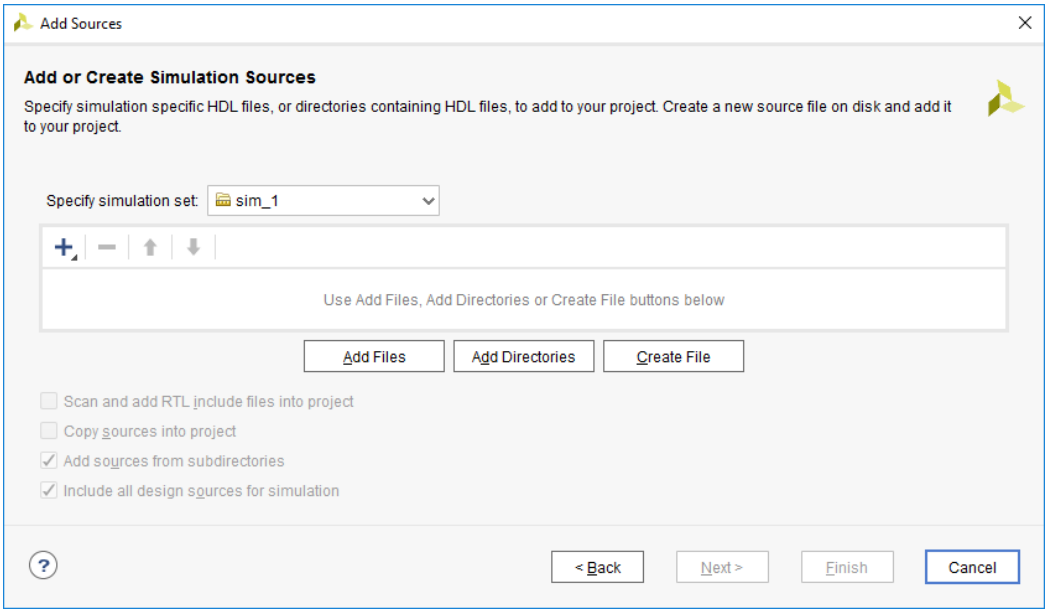
6. In the Navigator windows, click **Add Sources** again.



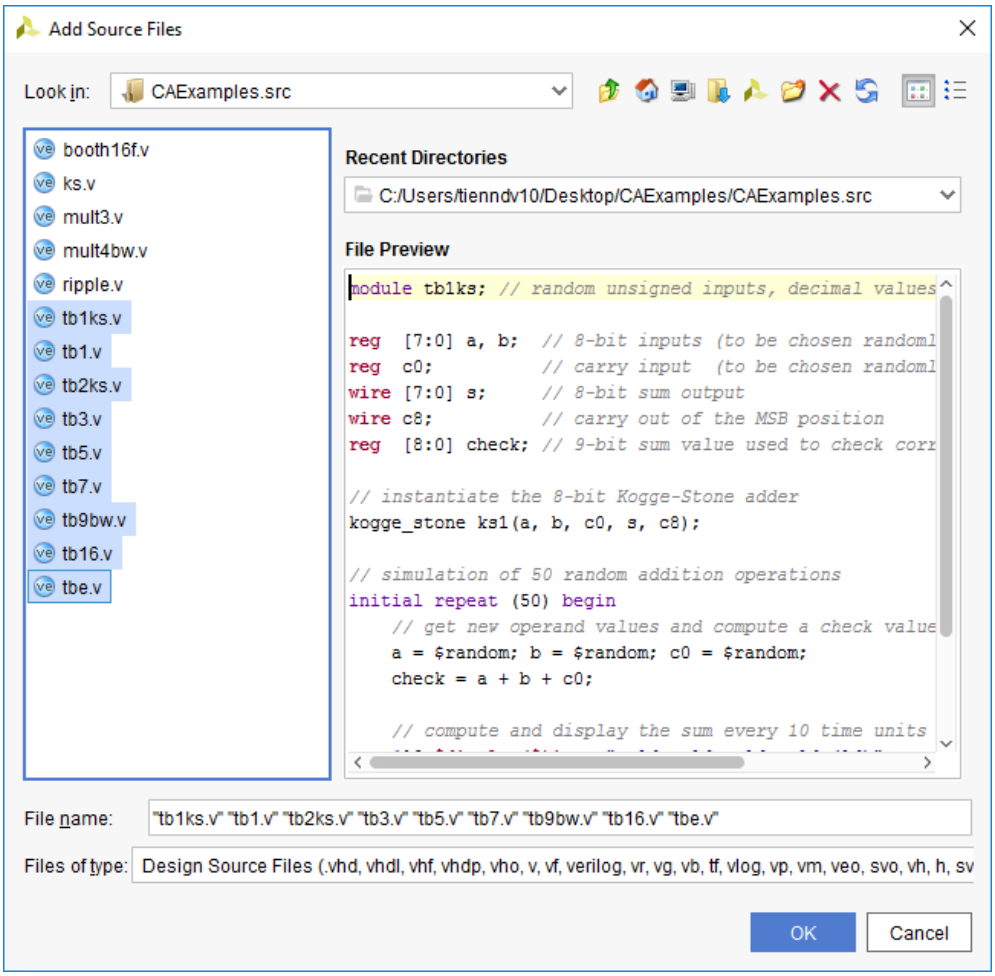
7. Select **Add or create simulation sources**. Click **Next**.



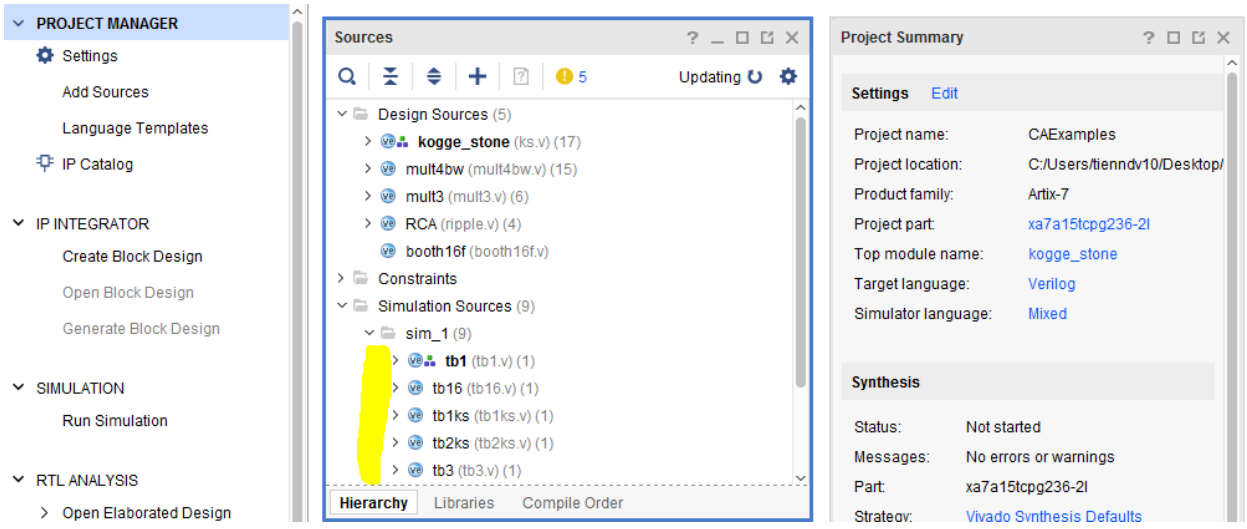
8. Click **Add Files**.



9. Select all testbench files you has downloaded. Click **OK**.



10. Click **Finish**. The project as below

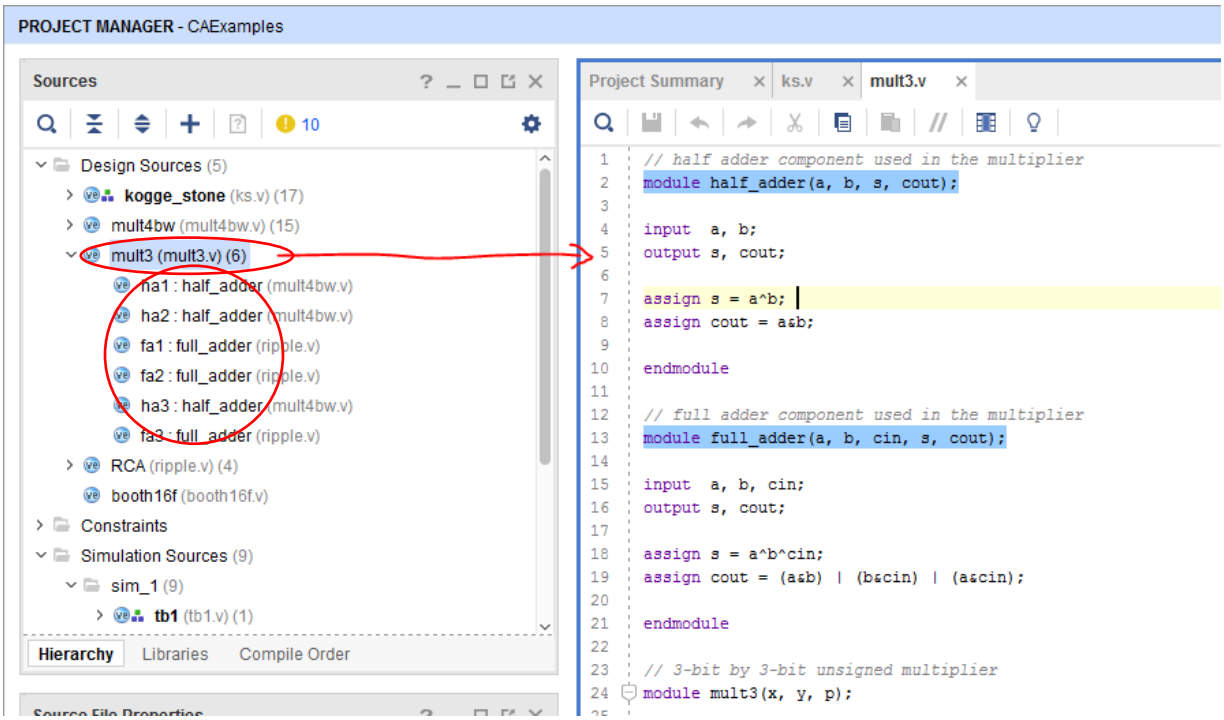


View source, RTL, and Simulation

View source

Click filename at **Sources** windows, and view the source at the right editor

In the sample image below, the module's name is **mult3. mult3** includes 3 submodules **halft_adder** with name ha1, ha2, ha3; and 3 submodules **full_adder** with name fa1, fa2, fa3.

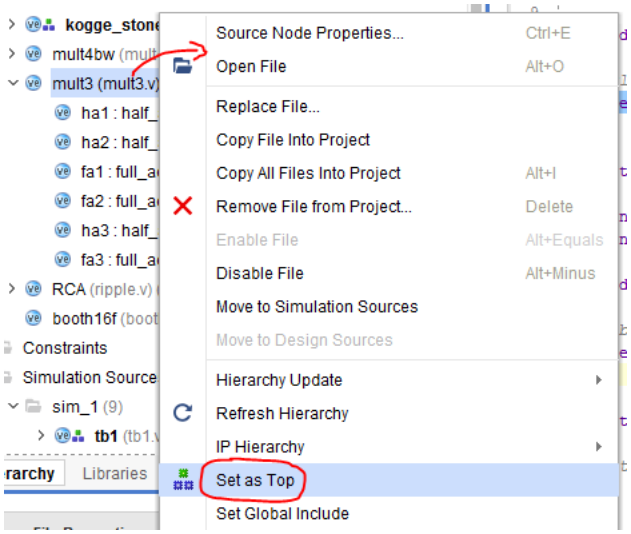


RTL Analysis

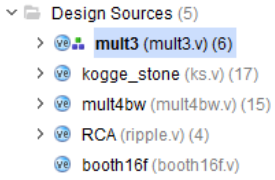
RTL means Register Transistor Level. With RTL, you can see the logic diagram of your design.

1. Because the design has so many modules, and because we could test just a part of design, so must choice the top module.

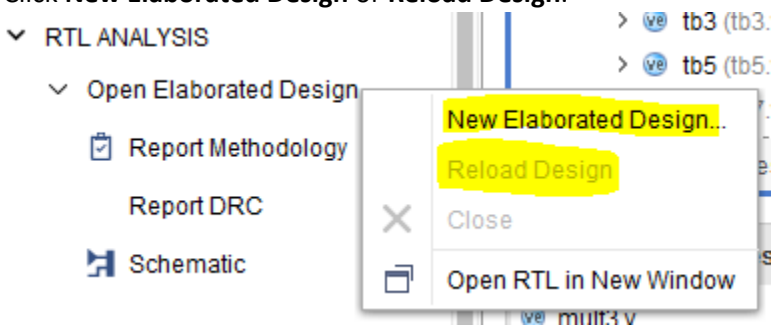
   Right click the selected module, and click **Set as Top.**

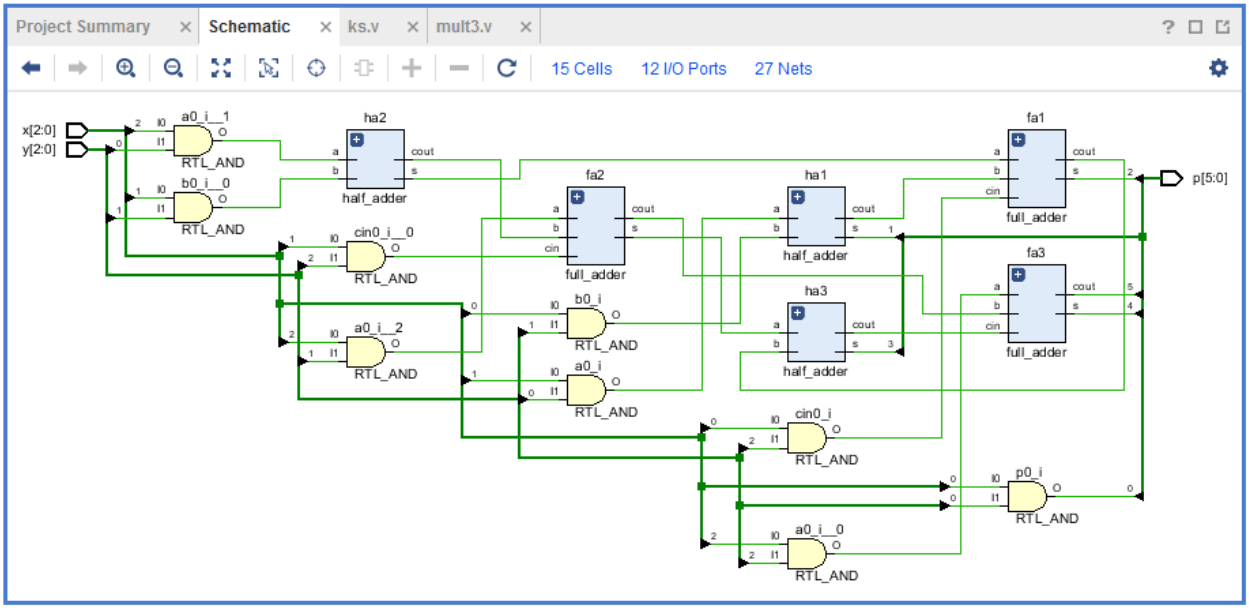
   After that, the module must be bold

2. In the **Navigation** window, click **Open Elaborated Design**.
   Click **New Elaborated Design** or **Reload Design**.



3. Wait in a few seconds.. and view the Schematic



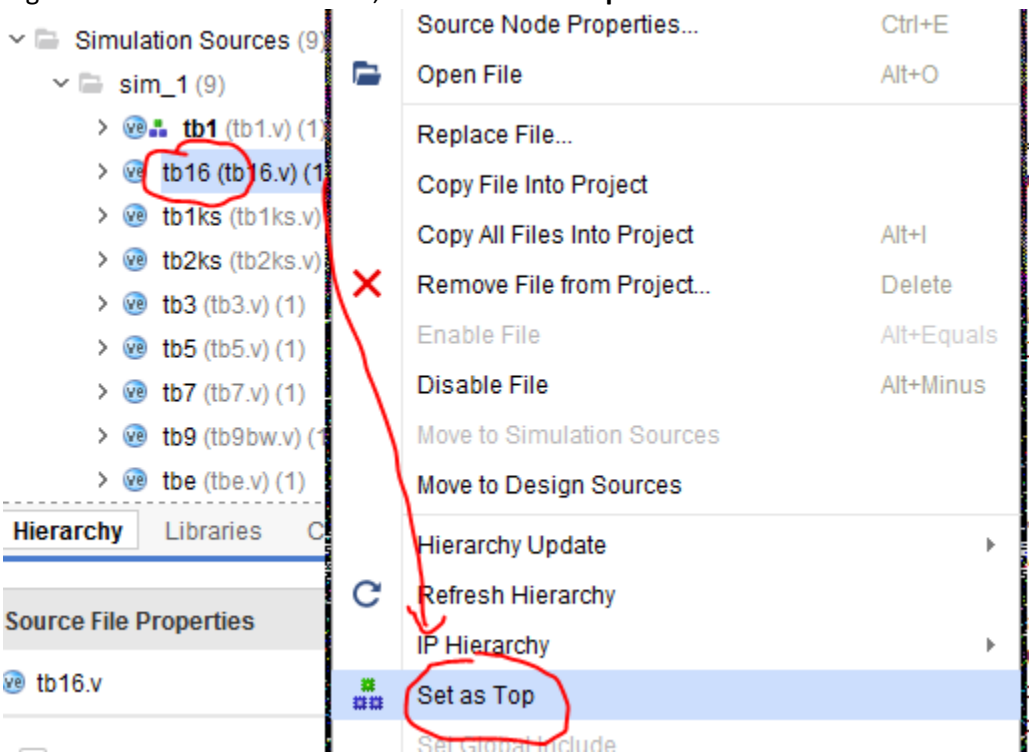
Simulation

Run testbench file.

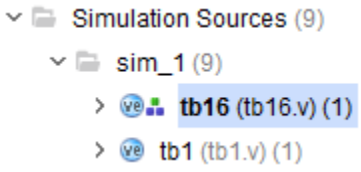
- Testbench defines stimulators for all inputs.
- The design calculates outputs.
- And the testbench verifies the outputs and expected results to make sure that the design is correct.

1. Because the design has so many testbench, and because we could test just a part of design, so must choice the top testbench.

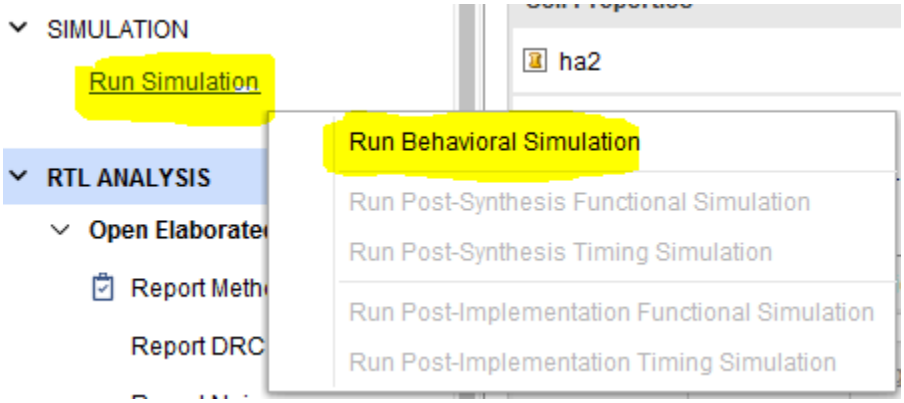
   Right click the selected module, and click **Set as Top.**



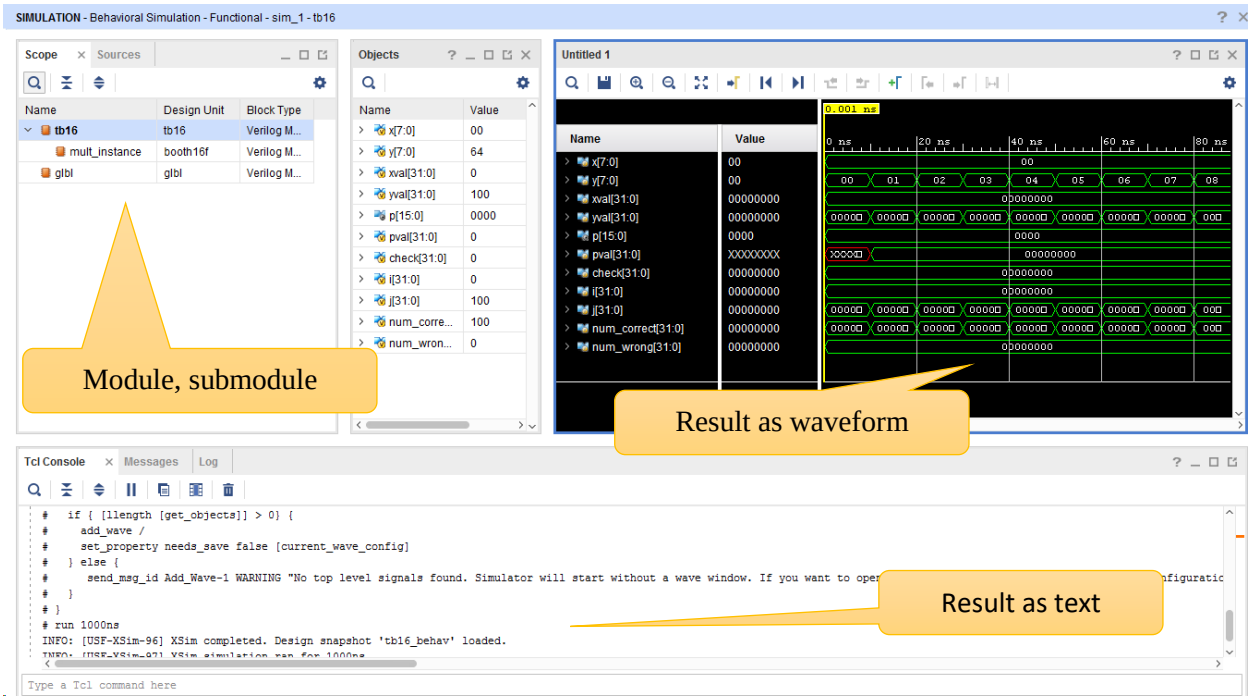
   After that, the testbench must be bold



2. In the **Navigation** window, click **Run Simulation**.
   Click **Run Behavioral Simulation**.



3. Wait in a few seconds.. and view the result



Zoom-in, zoom-out waveform to view better.

And run simulation in a certain time range.