

# Implementing design and testbench by Xilinx Vivado and SystemVerilog

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University of Minnesota

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Department of Computer Engineering,  
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## Install Xilinx Vivado

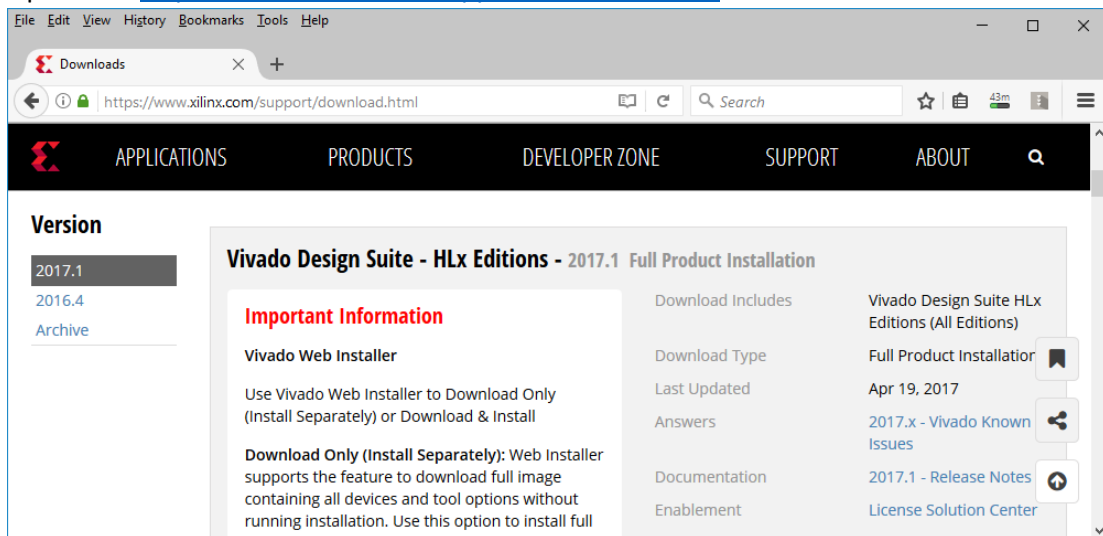
If you are at the laboratory at Ta Quang Buu library building, the software is available.

Just run the command below

```
$ /opt/Xilinx/Vivado/2017.1/bin/vivado
```

Otherwise, you could download and install Vivado:

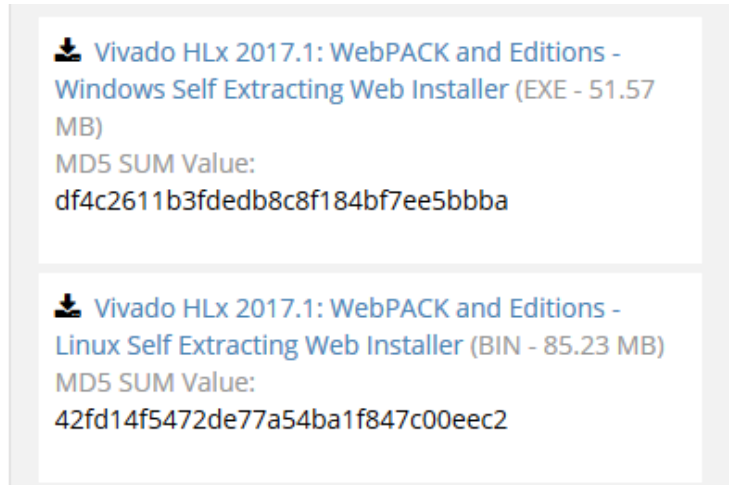
1. Create an free account at [www.xilinx.com](http://www.xilinx.com)
2. Open URL: <https://www.xilinx.com/support/download.html>



The screenshot shows a web browser window displaying the Xilinx support page for Vivado Design Suite - HLx Editions - 2017.1 Full Product Installation. The page includes a navigation menu with links for APPLICATIONS, PRODUCTS, DEVELOPER ZONE, SUPPORT, and ABOUT. The main content area features a 'Version' section with links for 2017.1, 2016.4, and Archive. The primary focus is on the 'Vivado Design Suite - HLx Editions - 2017.1 Full Product Installation' section, which contains 'Important Information' about the Vivado Web Installer and Download Only options. A table on the right lists details such as 'Download Includes', 'Download Type', 'Last Updated', 'Answers', 'Documentation', and 'Enablement'.

Download Includes	Vivado Design Suite HLx Editions (All Editions)
Download Type	Full Product Installer
Last Updated	Apr 19, 2017
Answers	<a href="#">2017.x - Vivado Known Issues</a>
Documentation	<a href="#">2017.1 - Release Notes</a>
Enablement	<a href="#">License Solution Center</a>

3. Scroll down to the middle and click **suitable installation package link**, for Windows or for Linux (all CentOS, Ubuntu... are okay)

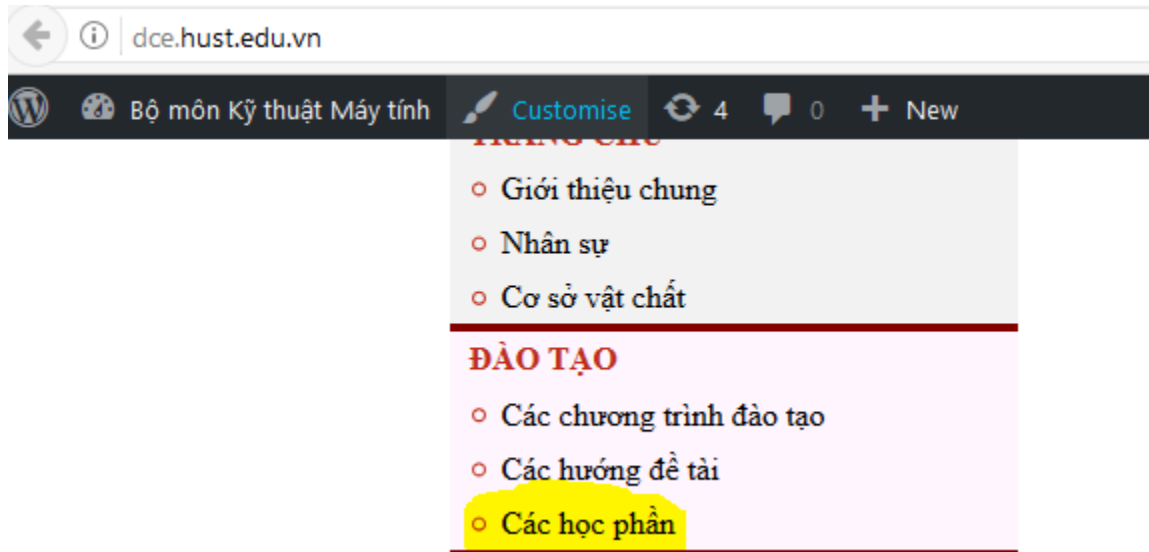


4. Install Vivado. It may take a few hours.  
Remember that: you should choice WebPack version. It's free licensing.

## Download Resources

Download slides and Verilog files

1. Open URL: <http://dce.hust.edu.vn>
2. At the left menu, click **Các học phần**



### 3. Open the post IT3282E – Computer Architecture: Content and References

doe.hust.edu.vn/it3282e-computer-architecture-content-and-references/

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- o Biểu mẫu

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- o Thông báo

## IT3282E – Computer Architecture: Content and References

15/05/2017 Gerald Sobelman Leave a comment



Prof. Gerald Sobelman

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Research Area: Computer Engineering, VLSI, and Circuits

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### Slides

1. [Adders](#)
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### 4. Download slides and verilog files

### Slides

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### Verilog Files for Simulation

Module	Testbench
1. <a href="#">booth16f</a>	1. <a href="#">tb1</a>
2. <a href="#">ks</a>	2. <a href="#">tb1ks</a>
3. <a href="#">mult3</a>	3. <a href="#">tb2ks</a>
4. <a href="#">mult4bw</a>	4. <a href="#">tb3</a>
5. <a href="#">ripple</a>	5. <a href="#">tb5</a>
	6. <a href="#">tb7</a>
	7. <a href="#">tb9bw</a>
	8. <a href="#">tb16</a>
	9. <a href="#">tbe</a>

# Create Project and add Verilog sources

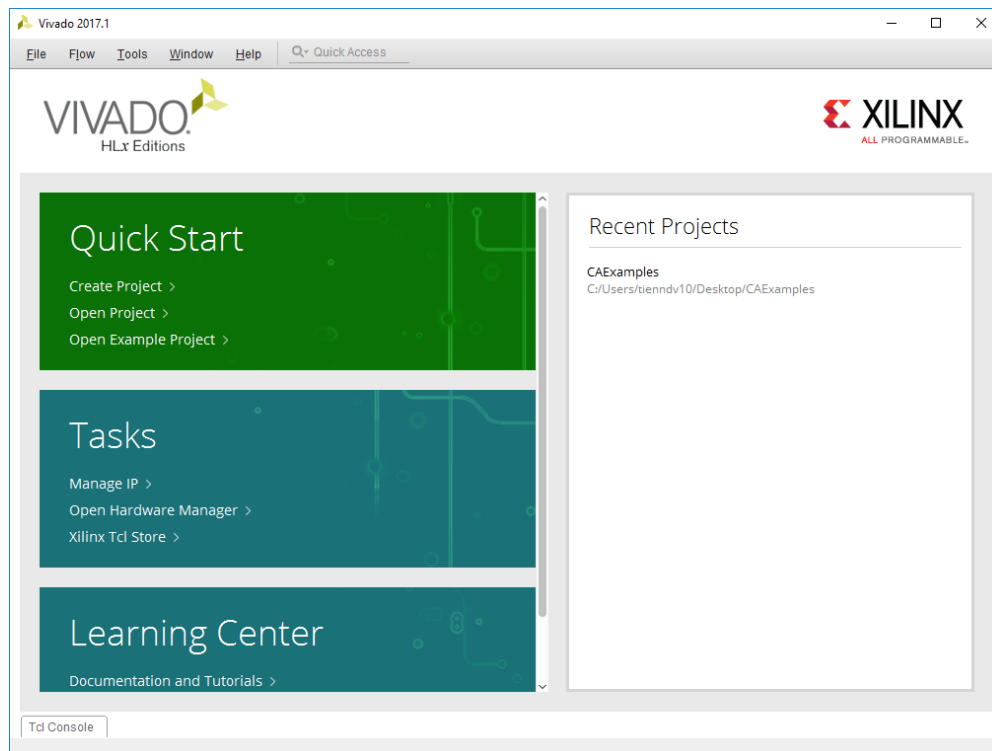
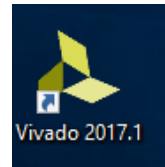
## Create Project

1. Run Vivado

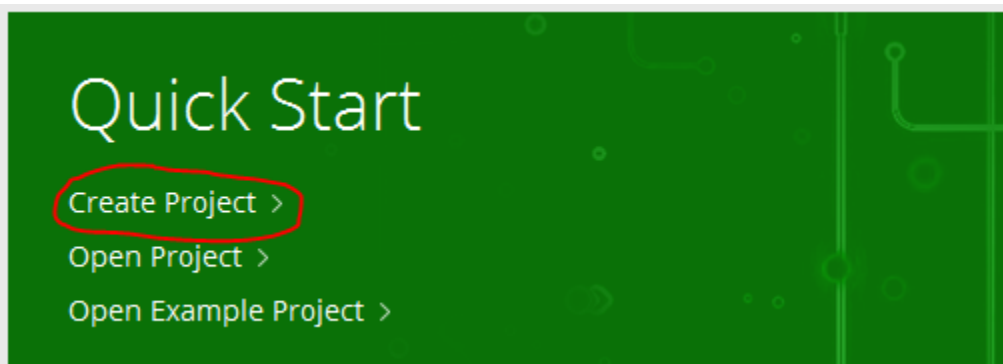
Linux:

```
$ /opt/Xilinx/Vivado/2017.1/bin/vivado
```

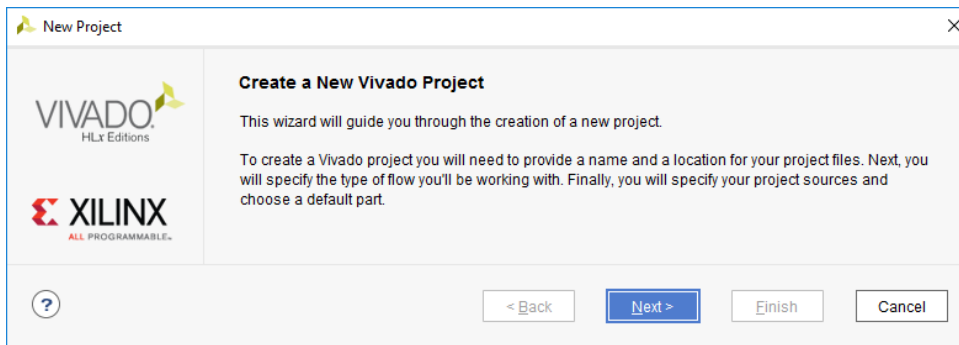
Windows: click **vivado icon**.



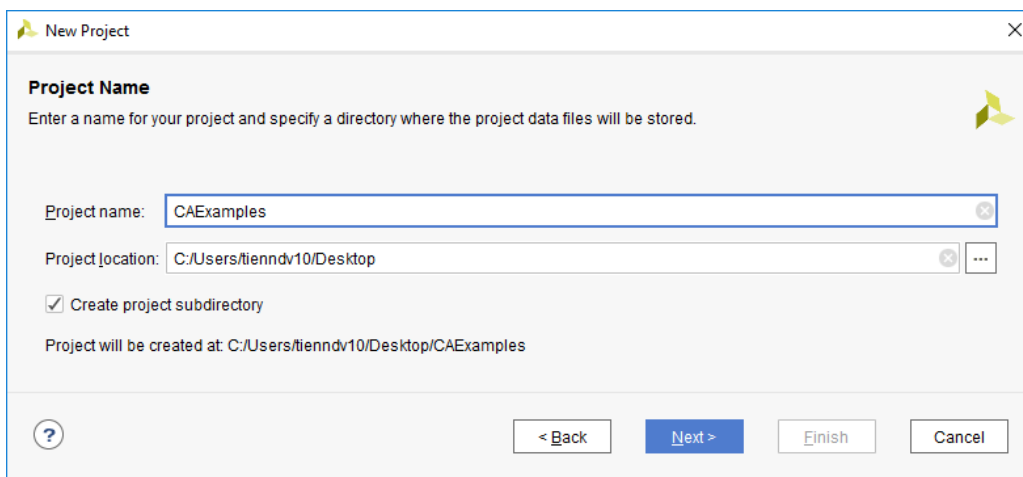
2. Click **Create New Project**.



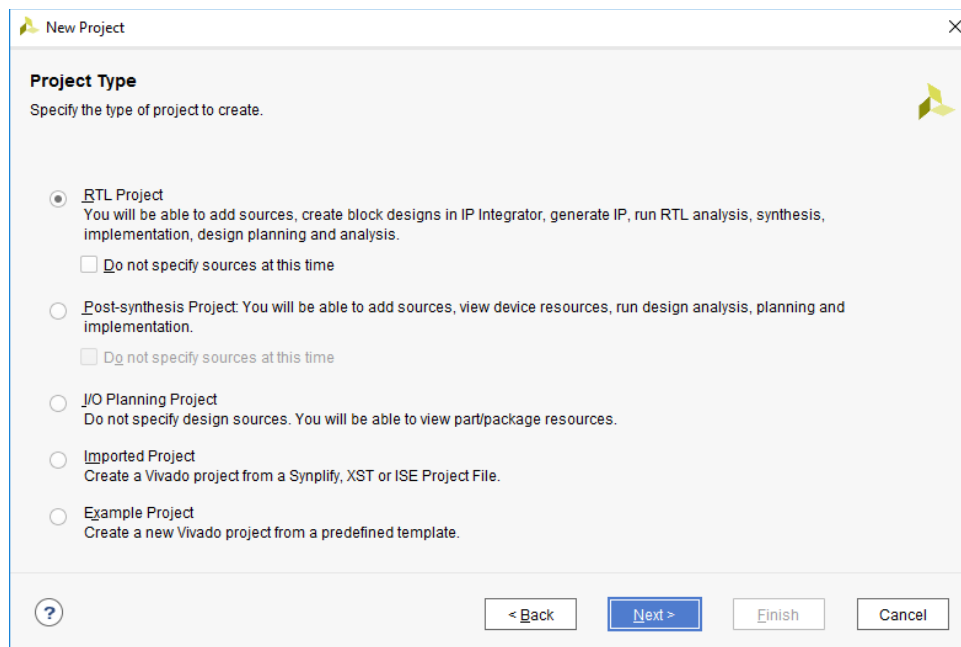
3. Click **Next**.



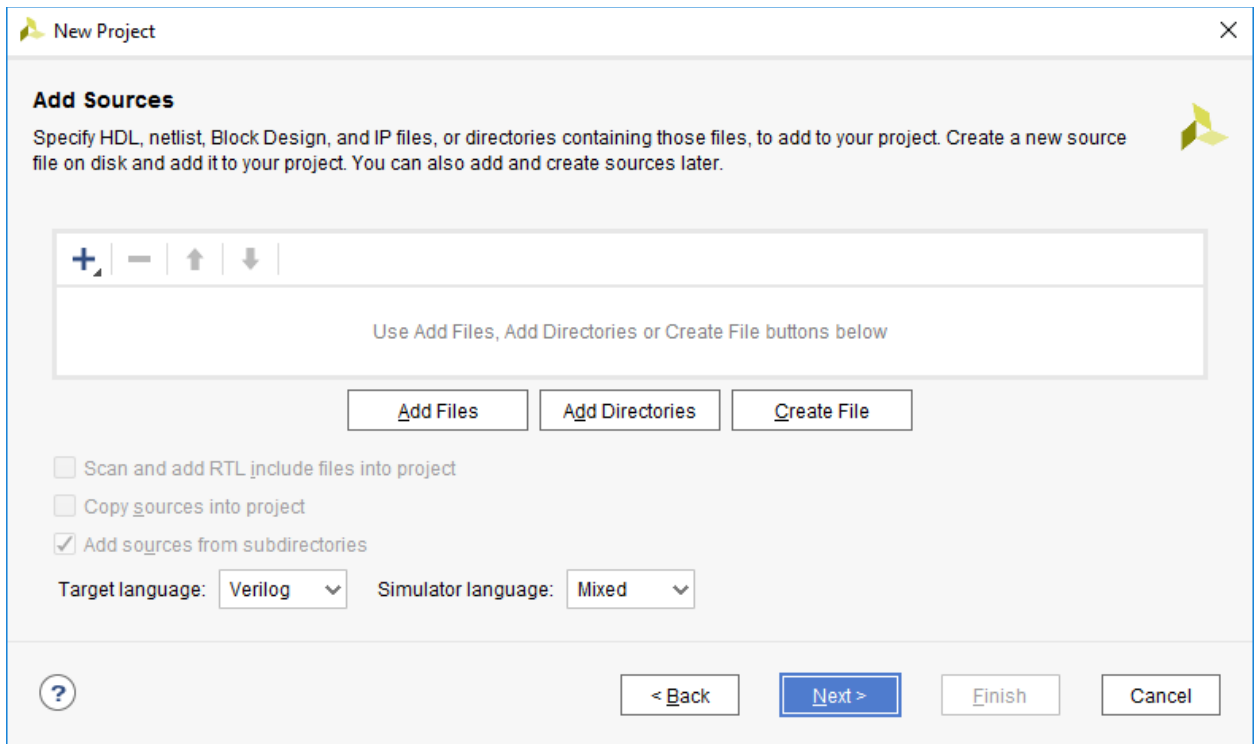
4. Name the project, for example CAExamples. Click **Next**.



5. At New Project dialog, make sure that **RTL Project** is selected, and don't choice **Do not specify sources at this time**. Click Next.

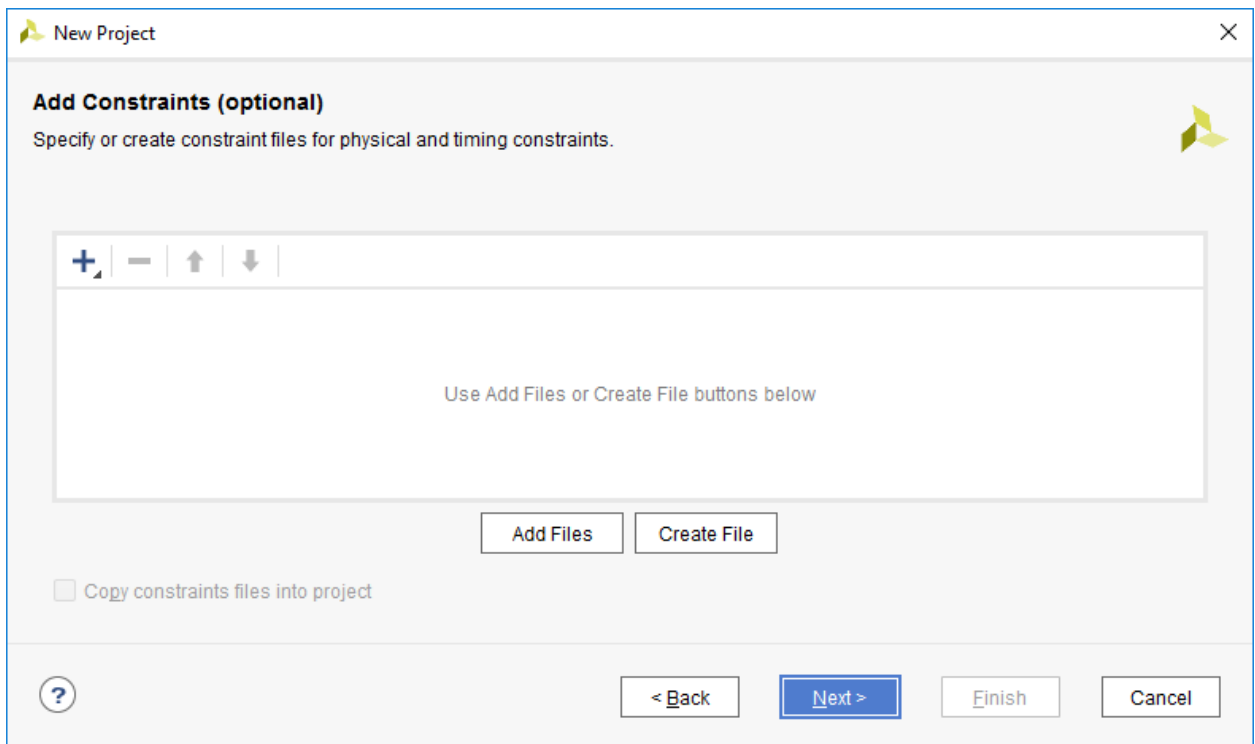


6. Target language should be **Verilog**. Click **Next**.



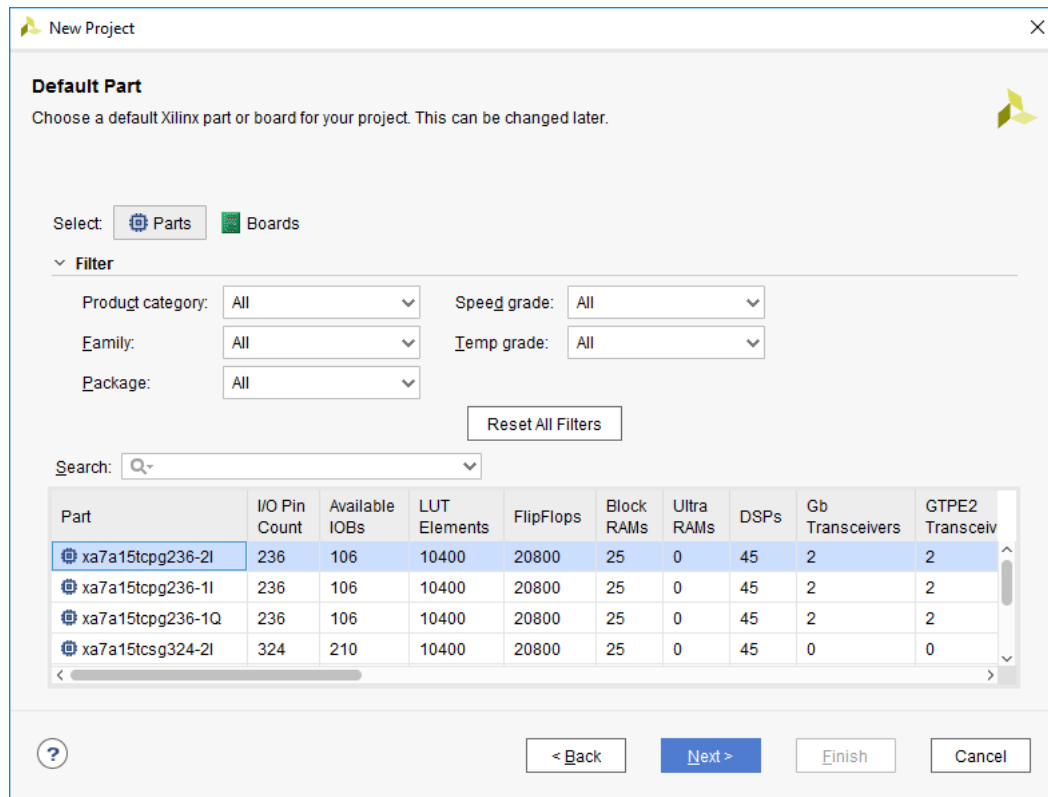
The screenshot shows the 'New Project' dialog box with the 'Add Sources' step selected. The title bar reads 'New Project' with a close button. The main heading is 'Add Sources'. Below it, a text block explains: 'Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.' To the right is a yellow logo. A large empty text area contains the instruction 'Use Add Files, Add Directories or Create File buttons below'. Below this are three buttons: 'Add Files', 'Add Directories', and 'Create File'. There are three checkboxes: 'Scan and add RTL include files into project' (unchecked), 'Copy sources into project' (unchecked), and 'Add sources from subdirectories' (checked). Below the checkboxes are two dropdown menus: 'Target language:' set to 'Verilog' and 'Simulator language:' set to 'Mixed'. At the bottom, there is a help icon (question mark in a circle), a '< Back' button, a 'Next >' button (highlighted in blue), a 'Finish' button, and a 'Cancel' button.

7. Click **Next**.

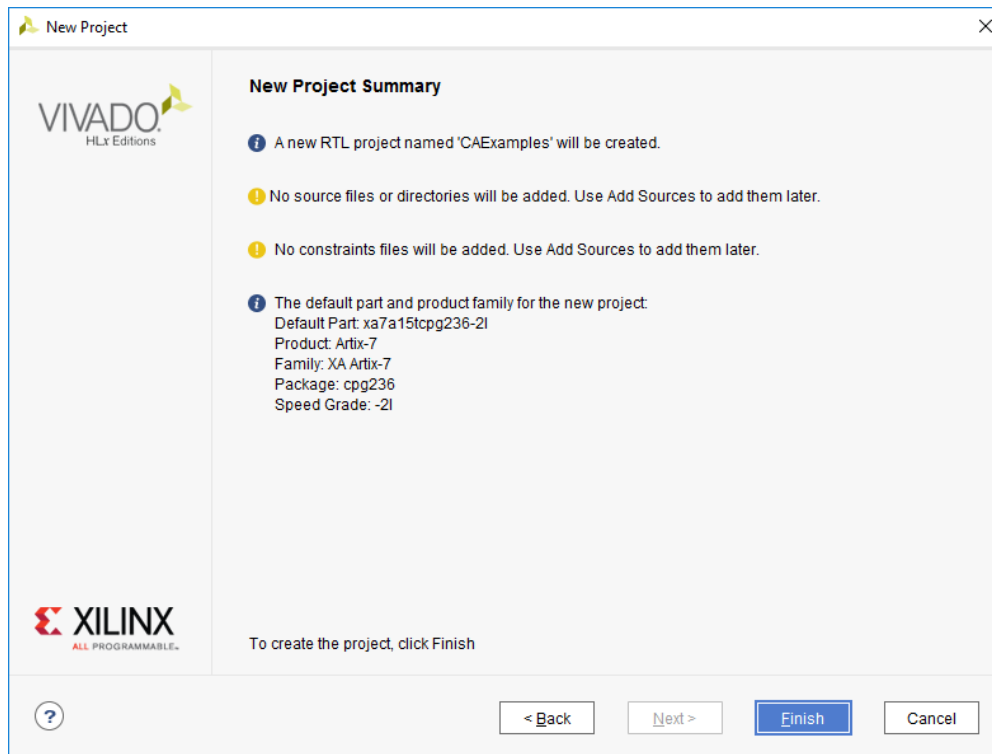


The screenshot shows the 'New Project' dialog box with the 'Add Constraints (optional)' step selected. The title bar reads 'New Project' with a close button. The main heading is 'Add Constraints (optional)'. Below it, a text block explains: 'Specify or create constraint files for physical and timing constraints.' To the right is a yellow logo. A large empty text area contains the instruction 'Use Add Files or Create File buttons below'. Below this are two buttons: 'Add Files' and 'Create File'. There is one checkbox: 'Copy constraints files into project' (unchecked). At the bottom, there is a help icon (question mark in a circle), a '< Back' button, a 'Next >' button (highlighted in blue), a 'Finish' button, and a 'Cancel' button.

8. Choice a certain FPGA, for example xa7a15tcbg236-2l. Click **Next**

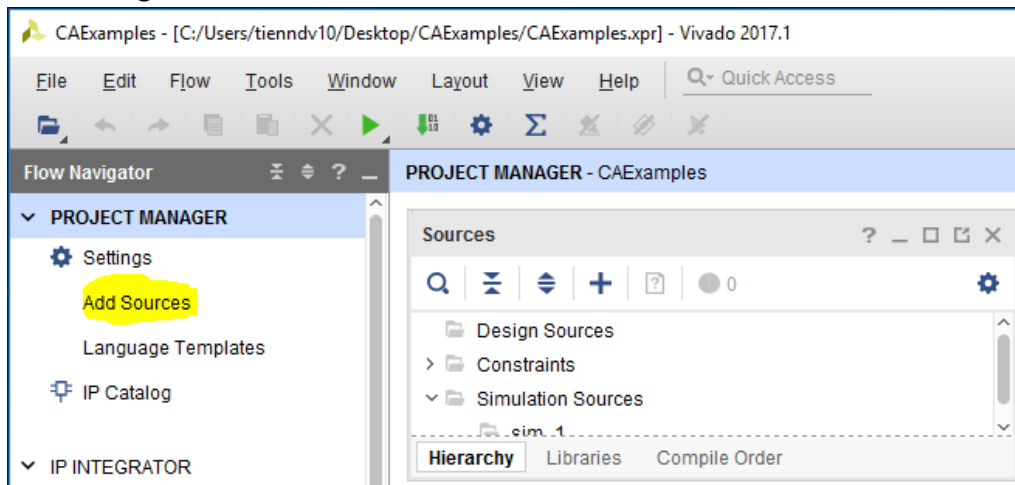


9. Click **Finish**.

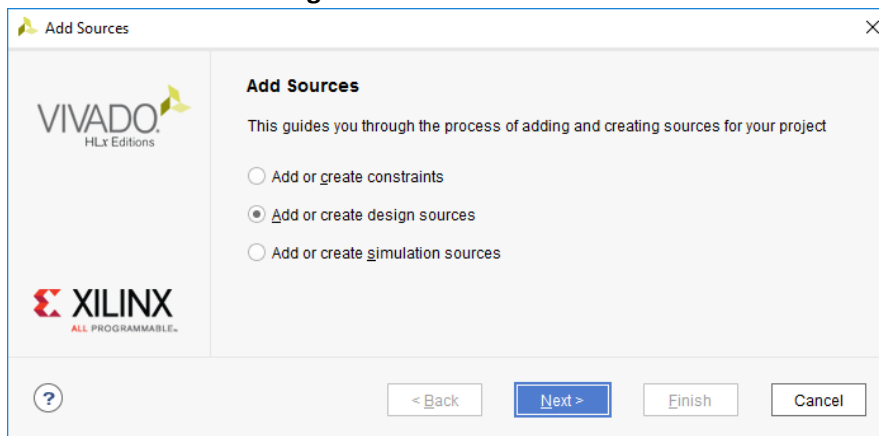


## Add Verilog sources

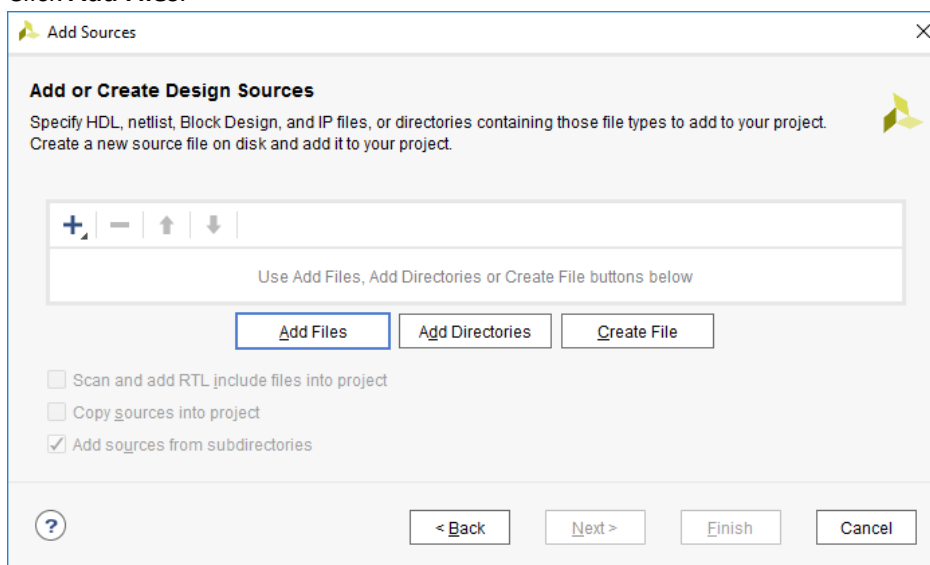
1. In the **Navigator** windows, click **Add Sources**.



2. Select **Add or create design sources**. Click **Next**.

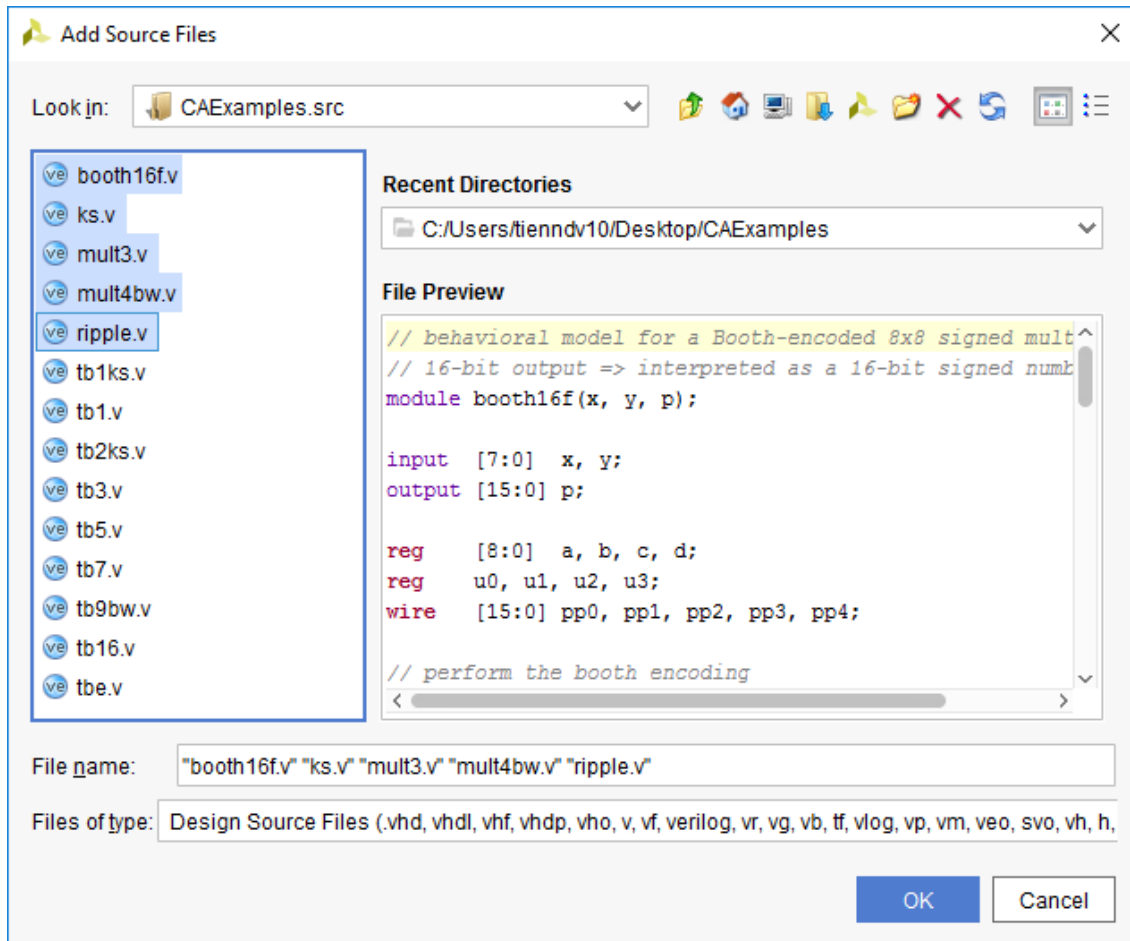


3. Click **Add Files**.

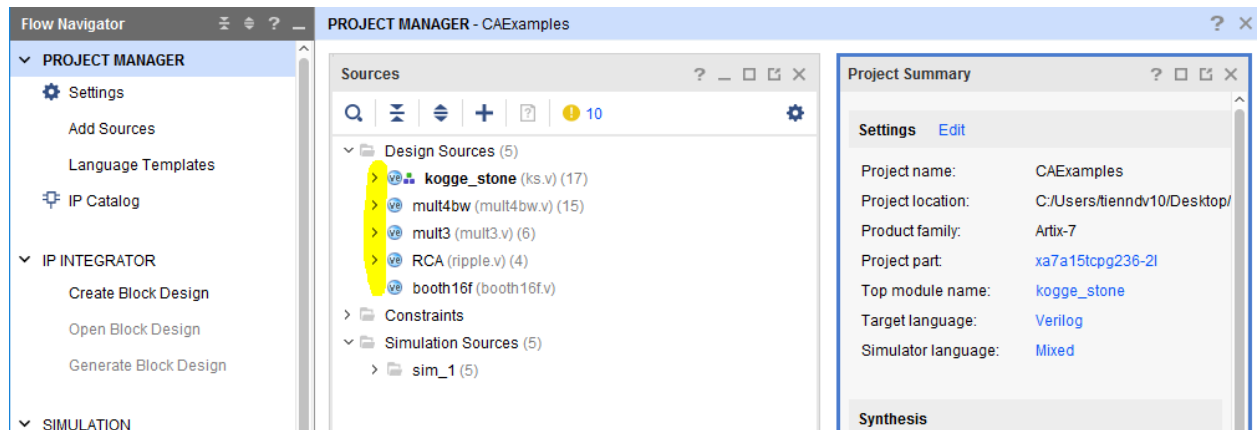




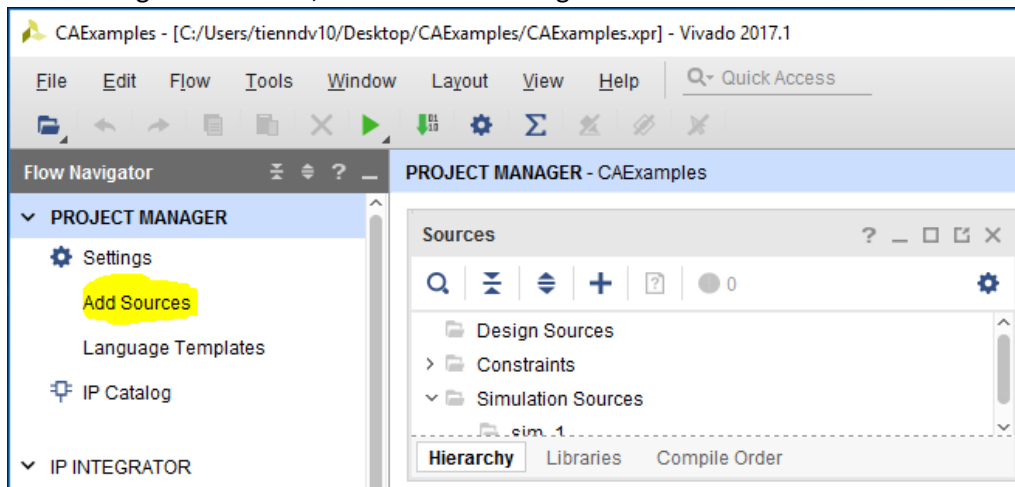
4. Select all module files you has downloaded, except testbench files (tb....v). Click **OK**.



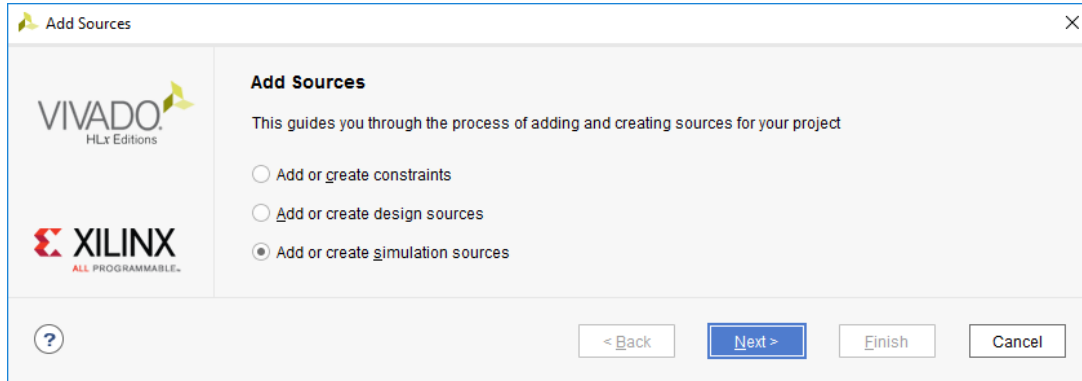
5. Click **Finish**. The project as below



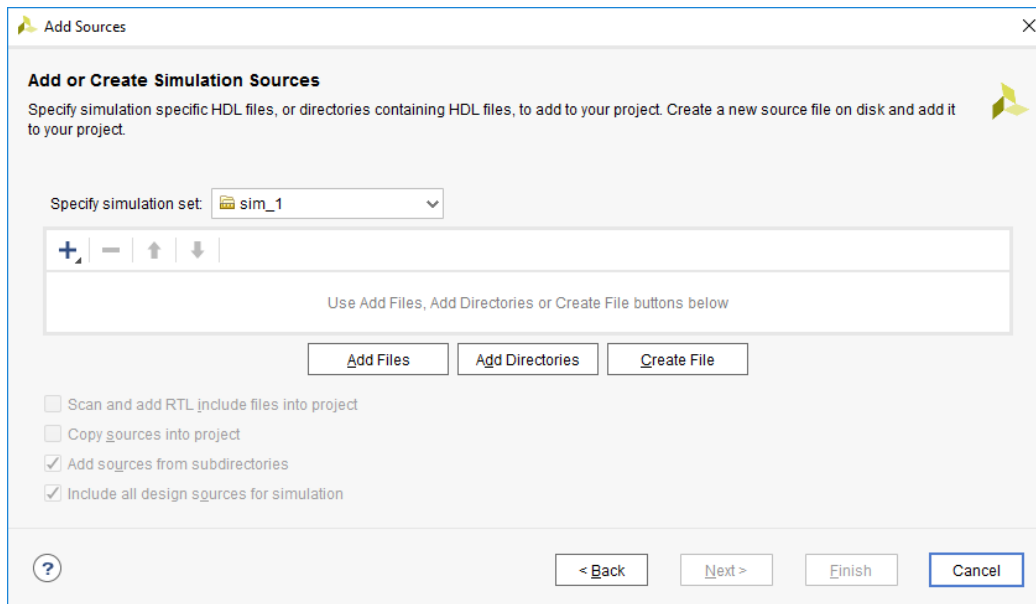
6. In the Navigator windows, click **Add Sources** again.



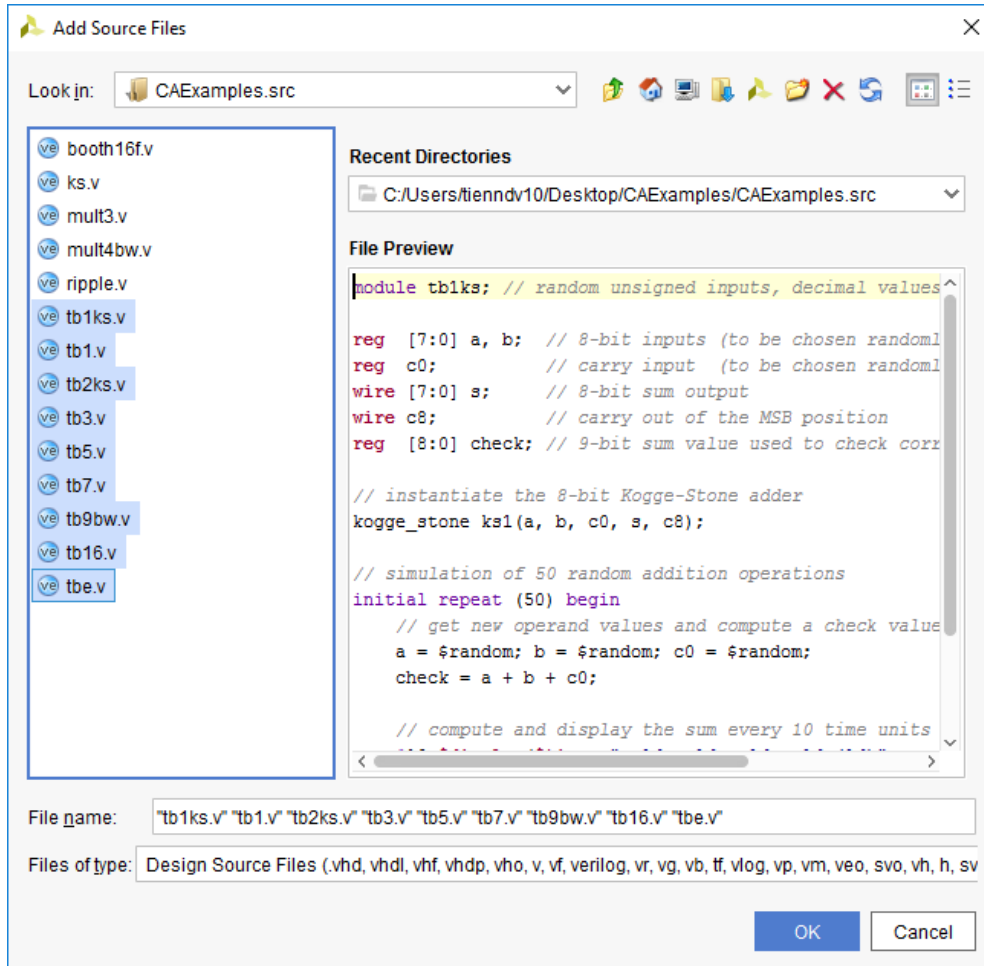
7. Select **Add or create simulation sources**. Click **Next**.



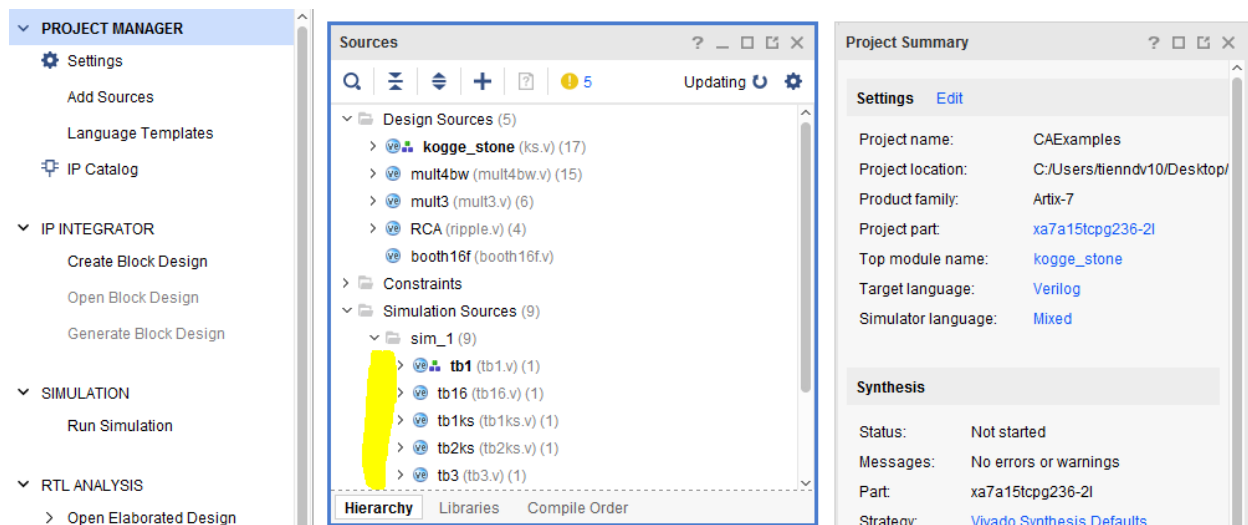
8. Click **Add Files**.



9. Select all testbench files you have downloaded. Click **OK**.



10. Click **Finish**. The project as below

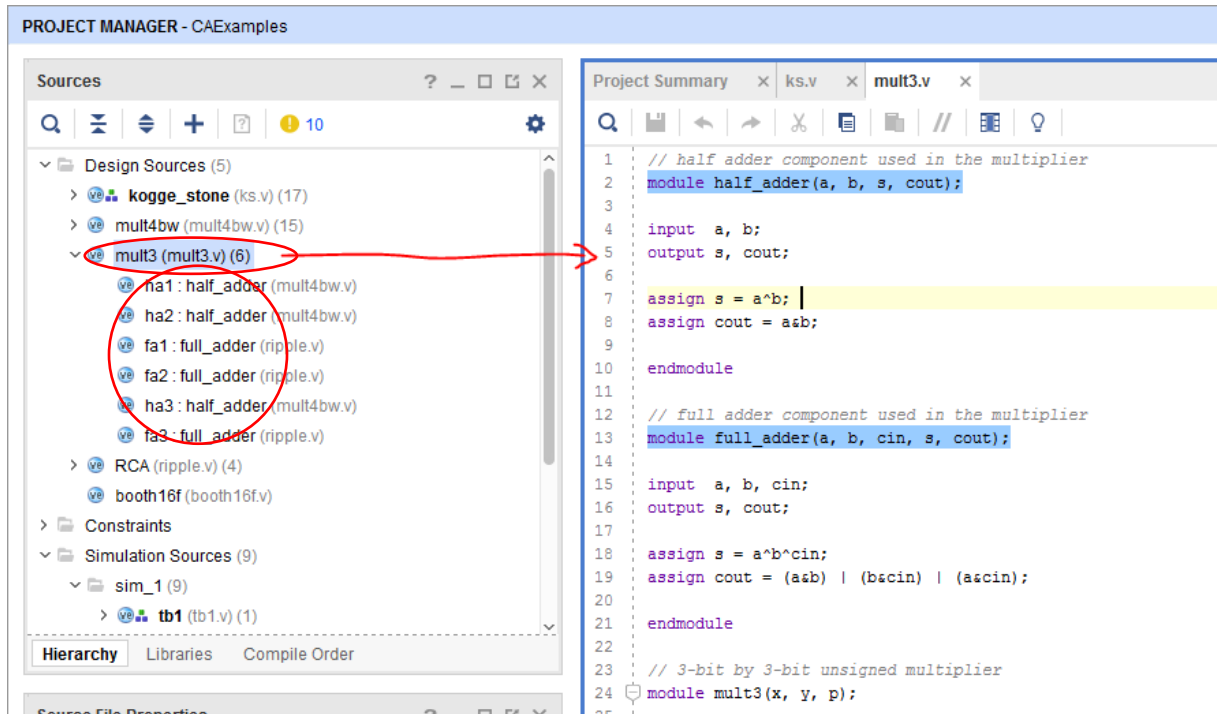


# View source, RTL, and Simulation

## View source

Click filename at **Sources** windows, and view the source at the right editor

In the sample image below, the module's name is **mult3**. **mult3** includes 3 submodules **half\_adder** with name ha1, ha2, ha3; and 3 submodules **full\_adder** with name fa1, fa2, fa3.



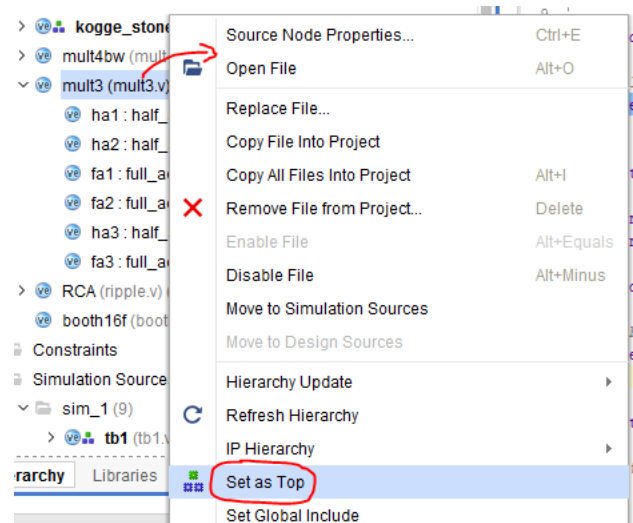
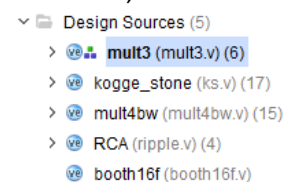
## RTL Analysis

RTL means Register Transistor Level. With RTL, you can see the logic diagram of your design.

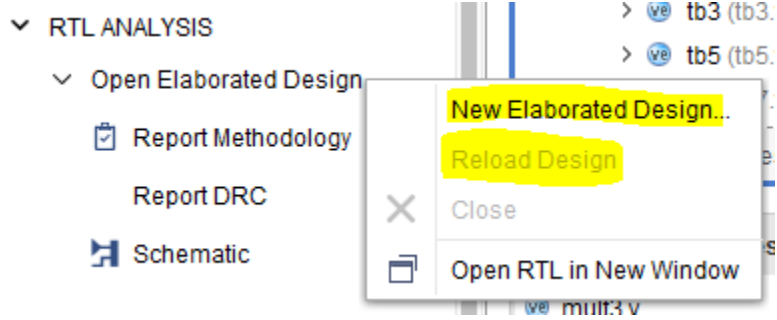
1. Because the design has so many modules, and because we could test just a part of design, so must choice the top module.

Right click the selected module, and click **Set as Top**.

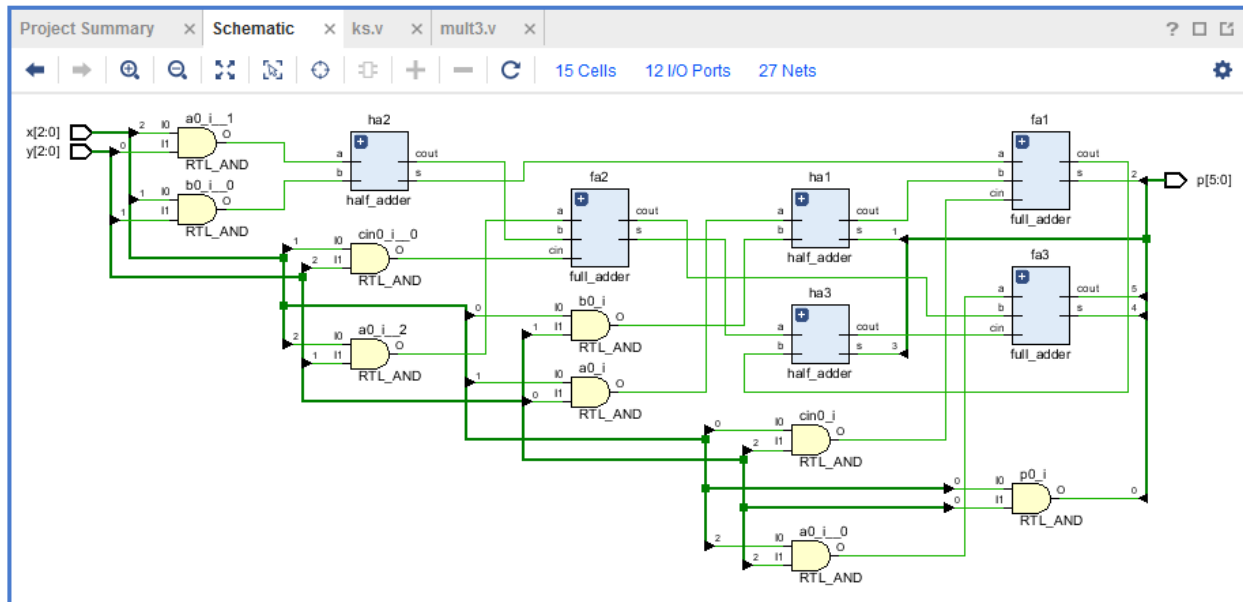
After that, the module must be bold



2. In the **Navigation** window, click **Open Elaborated Design**.  
Click **New Elaborated Design** or **Reload Design**.



3. Wait in a few seconds.. and view the Schematic



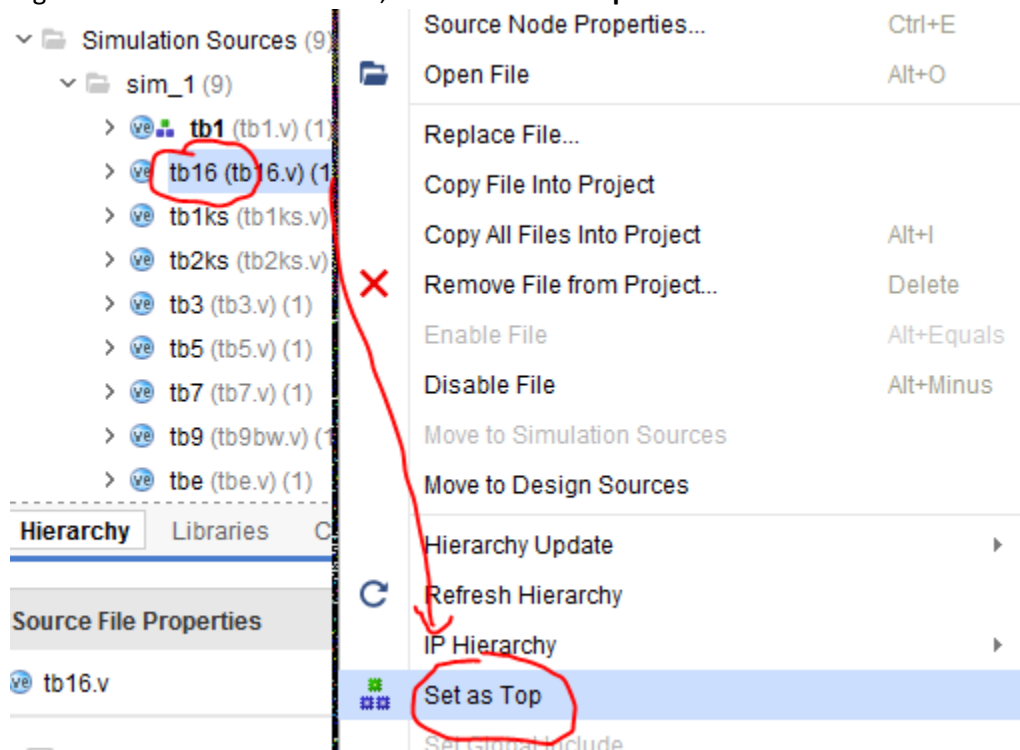
## Simulation

Run testbench file.

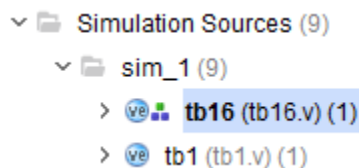
- Testbench defines stimulators for all inputs.
- The design calculates outputs.
- And the testbench verifies the outputs and expected results to make sure that the design is correct.

1. Because the design has so many testbench, and because we could test just a part of design, so must choice the top testbench.

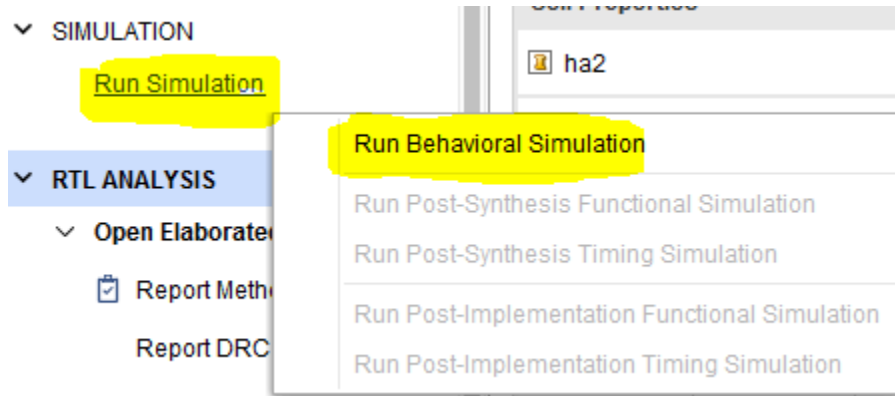
Right click the selected module, and click **Set as Top**.



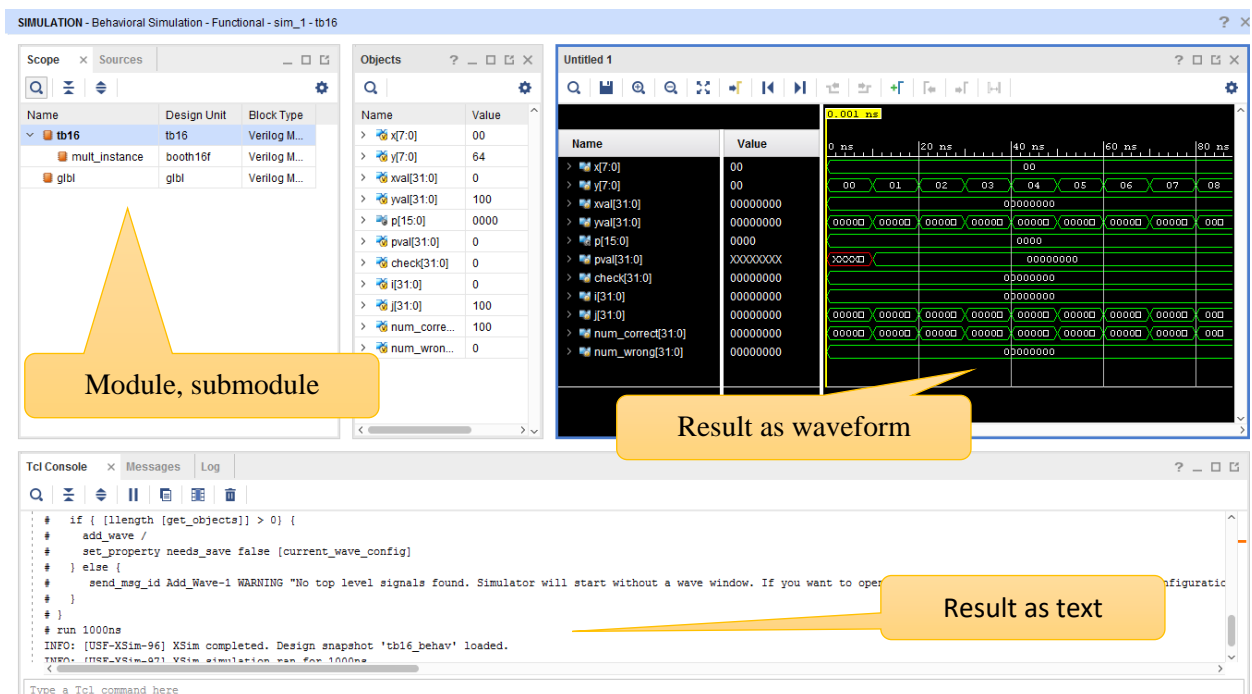
After that, the testbench must be bold



- In the **Navigation** window, click **Run Simulation**.  
Click **Run Behavioral Simulation**.



- Wait in a few seconds.. and view the result



Zoom-in, zoom-out waveform to view better.

And run simulation in a certain time range.

