Implementing design and testbench by Xilinx Vivado and SystemVerilog

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Install Xilinx Vivado

If you are at the laboratory at Ta Quang Buu library building, the software is available.

Just run the command below

\$ /opt/Xilinx/Vivado/2017.1/bin/vivado

Otherwise, you could download and install Vivado:

- 1. Create an free account at <u>www.xilinx.com</u>
- 2. Open URL: <u>https://www.xilinx.com/support/download.html</u> <u>Eile Edit View Higtory Bookmarks Tools Help</u>



3. Scroll down to the middle and click **suitable installation package link**, for Windows or for Linux (all CentOS, Ubuntu... are okay)

 Vivado HLx 2017.1: WebPACK and Editions -Windows Self Extracting Web Installer (EXE - 51.57 MB) MD5 SUM Value: df4c2611b3fdedb8c8f184bf7ee5bbba
 Vivado HLx 2017.1: WebPACK and Editions -Linux Self Extracting Web Installer (BIN - 85.23 MB) MD5 SUM Value: 42fd14f5472de77a54ba1f847c00eec2

4. Install Vivado. It may take a few hours. Remember that: you should choice WebPack version. It's free licensing.

Download Resources

Download slides and Verilog files

- 1. Open URL: <u>http://dce.hust.edu.vn</u>
- 2. At the left menu, click Các học phần



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3. Open the post IT3282E – Computer Architecture: Content and References

4. Download slides and verilog files

Slides		
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5. VerilogExamples		
6. WallaceTrees		
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Module 1. booth16f 2. ks 3. mult3 4. mult4bw 5. ripple	Testbench 1. tb1 2. tb1ks 3. tb2ks 4. tb3 5. tb5 6. tb7 7. tb9bw 8. tb16	

Create Project and add Verilog sources

Create Project

- 1. Run Vivado
 - Linux:





Windows: click vivado icon.



2. Click Create New Project.



3. Click Next.

🝌 New Project		×
HLX Editions	Create a New Vivado Project This wizard will guide you through the creation of a new project. To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.	
?	< <u>Back</u> <u>Next></u> <u>Finish</u> Cancel	

4. Name the project, for example CAExamples. Click Next.

🝌 New Project		×
Project Name Enter a name for yo	our project and specify a directory where the project data files will be stored.	A
Project name:	CAExamples	\otimes
Project location:	C:/Users/tienndv10/Desktop	⊗
✓ Create proje	ct subdirectory	
Project will be cr	eated at: C:/Users/tienndv10/Desktop/CAExamples	
?	< <u>B</u> ack <u>N</u> ext> <u>F</u> inish	Cancel

5. At New Project dialog, make sure that **RTL Project** is selected, and don't choice **Do not specify sources at this time.** Click Next.



6. Target language should be Verilog. Click Next.

💫 New Project	×
Add Sources Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.	4
$ +_{\lambda} = + + $	
Use Add Files, Add Directories or Create File buttons below	
Add Files Add Directories Create File	
Scan and add RTL include files into project	
Copy sources into project	
Add sources from subdirectories	
Target language: Verilog 🗸 Simulator language: Mixed 🗸	
A Back <u>Next></u> <u>Finish</u> Ca	ncel

7. Click Next.

🚴 New Project	X
Add Constraints (optional) Specify or create constraint files for physical and timing constraints.	4
$ \mathbf{+}_{\mathbf{i}} = + + $	
Use Add Files or Create Fi	le buttons below
Add Files C	reate File
(?)	<u>ack Next > Einish Cancel</u>

8. Choice a certain FPGA, for example xa7a15tcpg236-2l. Click Next

🍌 New Project									×
Default Part Choose a default Xilinx pa Select: Parts ~ Filter	rt or board fo	r your project.	This can be	changed lat	er.				A
Product category:	All	~	Speed	grade: All			~		
Eamily:	All V Iemp grade: All V								
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Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Gb Transceivers	GTPE2 Transceiv
xa7a15tcpg236-2I	236	106	10400	20800	25	0	45	2	2
xa7a15tcpg236-11	236	106	10400	20800	25	0	45	2	2
xa7a15tcpg236-1Q	236	106	10400	20800	25	0	45	2	2
xa7a15tcsg324-2I	324	210	10400	20800	25	0	45	0	0 ~
<		_							>
?				< <u>B</u> ac	k	<u>N</u> ext :	>	Einish	Cancel

9. Click Finish.



Add Verilog sources

1. In the Navigator windows, click Add Sources.

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Add Sources		•
Language Templates	 Design Sources Constraints 	Î
₽ IP Catalog	~ 🗁 Simulation Sources	
✓ IP INTEGRATOR	Hierarchy Libraries Compile Order	×

Select Add or create design sources. Click Next.

À Add Sources		×
HLx Editions.	Add Sources This guides you through the process of adding and creating sources for your project	
	○ Add or <u>c</u> reate constraints	
	● <u>A</u> dd or create design sources	
	○ Add or create <u>s</u> imulation sources	
EXILINX ALL PROGRAMMABLE.		
(?)	< Back Lext > Einish Cancel	

3. Click Add Files.

Add Sources	×
Add or Create Design Sources Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.	4
+ - + Use Add Files, Add Directories or Create File buttons below	
Add Files Add Directories Create File	
 Scan and add RTL include files into project Copy sources into project Add sources from subdirectories 	
(?) < <u>B</u> ack <u>N</u> ext > <u>F</u> inish C	Cancel

4. Select all module files you has downloaded, except testbench files (tb....v). Click OK.



5. Click Finish. The project as below



6. In the Navigator windows, click **Add Sources** again.

🙏 CAExamples - [C:/Users/tienndv10/Deskt	op/CAExamples/CAExamples.xpr] - Vivado 2017.1	
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7. Select Add or create simulation sources. Click Next.

À Add Sources	×
	Add Sources This guides you through the process of adding and creating sources for your project
E XILINX ALL PROGRAMMABLE.	 Add or create constraints Add or create design sources Add or create simulation sources
?	< <u>Back</u> <u>Finish</u> Cancel

8. Click Add Files.

À Add Sources	×
Add or Create Simulation Sources Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.	2
Specify simulation set	
$ +_{z} = + + $	
Use Add Files, Add Directories or Create File buttons below	
Add Files Add Directories Create File	
Scan and add RTL include files into project	
Copy sources into project	
✓ Add sources from subdirectories	
✓ Include all design sources for simulation	

9. Select all testbench files you has downloaded. Click **OK**.



10. Click Finish. The project as below



View source, RTL, and Simulation

View source

Click filename at Sources windows, and view the source at the right editor

In the sample image below, the module's name is **mult3**. **mult3** includes 3 submodules **halft_adder** with name ha1, ha2, ha3; and 3 submodules **full_adder** with name fa1, fa2, fa3.



RTL Analysis

RTL means Register Transistor Level. With RTL, you can see the logic diagram of your design.

 Because the design has so many modules, and because we could test just a part of design, so must choice the top module.

Right click the selected module, and click **Set as Top.**

After that, the module must be bold

- Design Sources (5)
 @. mult3 (mult3.v) (6)
 @ kogge_stone (ks.v) (17)
 @ mult4bw (mult4bw.v) (15)
 @ RCA (ripple.v) (4)
 - mult4bw (mult4bw.v) (15)
 RCA (ripple.v) (4)
 booth16f (booth16f.v)



2. In the Navigation window, click Open Elaborated Design. Click New Elaborated Design or Reload Design.



3. Wait in a few seconds.. and view the Schematic



Simulation

Run testbench file.

- Testbench defines stimulators for all inputs.
- The design calculates outputs.
- And the testbench verifies the outputs and expected results to make sure that the design is correct.
- 1. Because the design has so many testbench, and because we could test just a part of design, so must choice the top testbench.



Right click the selected module, and click Set as Top.

After that, the testbench must be bold

Simulation Sources (9)
 sim_1 (9)
 tb16 (tb16.v) (1)
 tb1 (tb1.v) (1)

2. In the Navigation window, click Run Simulation. Click Run Behavioral Simulation.

✓ SIMULATION	a ha2							
	Run Behavioral Simulation							
✓ RTL ANALYSIS	Run Post-Synthesis Functional Simulation							
 Open Elaborate 	Due Dest Outbasis Timing Orgulation							
🛱 Report Meth	Run Post-Synthesis Timing Simulation							
E Report mean	Run Post-Implementation Functional Simulation							
Report DRC	Run Post-Implementation Timing Simulation							

3. Wait in a few seconds.. and view the result

SIMULATION - Behavioral S	imulation - Funct	tional - sim_1 - tb1	6										? >
Scope × Sources		_ 0 6	Objects ?	_ 🗆 🗆 ×	Untitled 1							?[) C X
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<pre># run 1000ns INFO: [USF-XSim-9] INFO: [USF-VSim_0] (ISF-VSim_0] (ISF-VSim_0] (ISF-VSim_0] (ISF-VSim_0] (ISF-VSim_0) (</pre>	6] XSim compl 71 VSim eimul here	eted. Design so	napshot 'tb16_behav'	loaded.									>

Zoom-in, zoom-out waveform to view better.

And run simulation in a certain time range.

